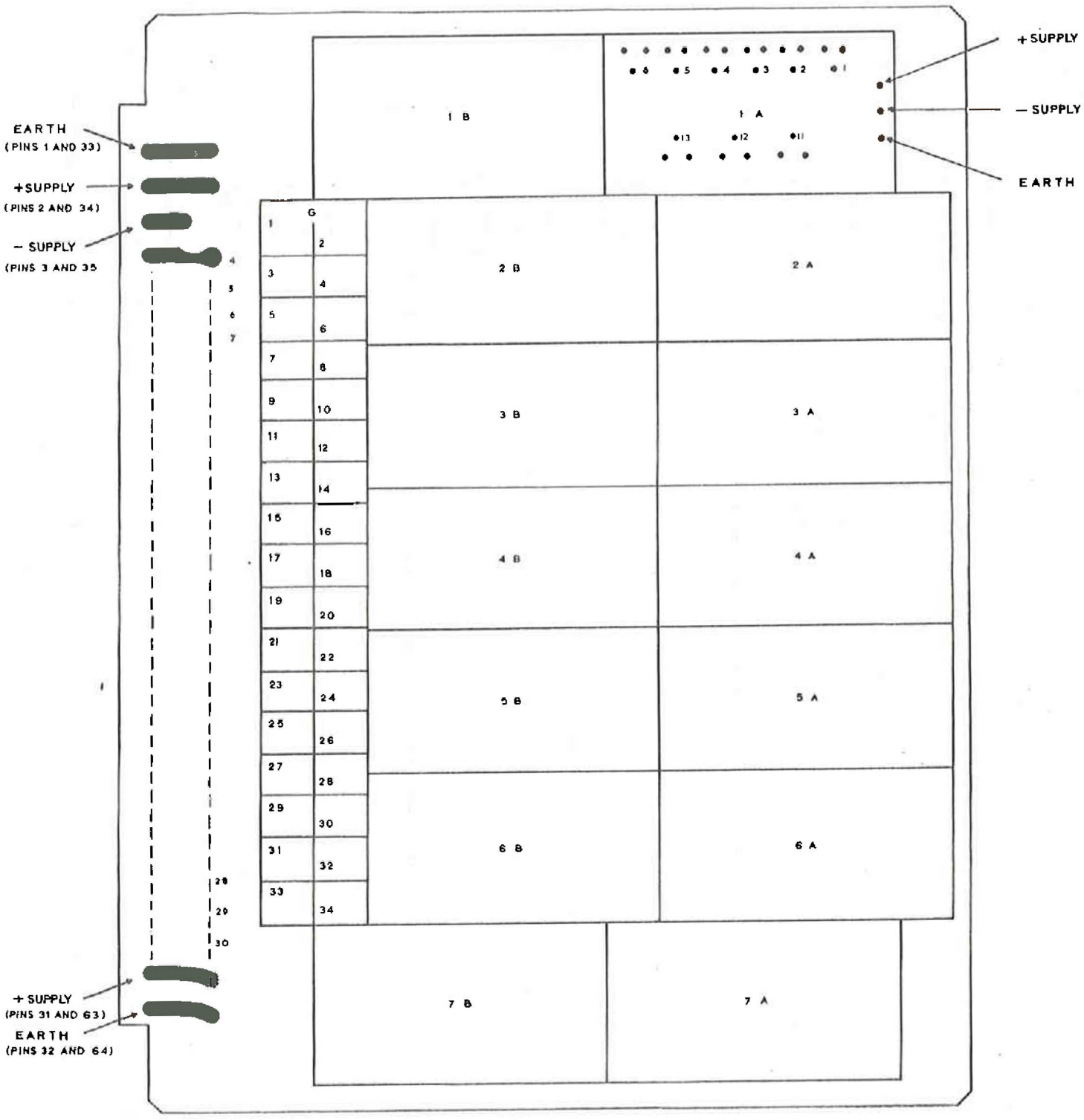


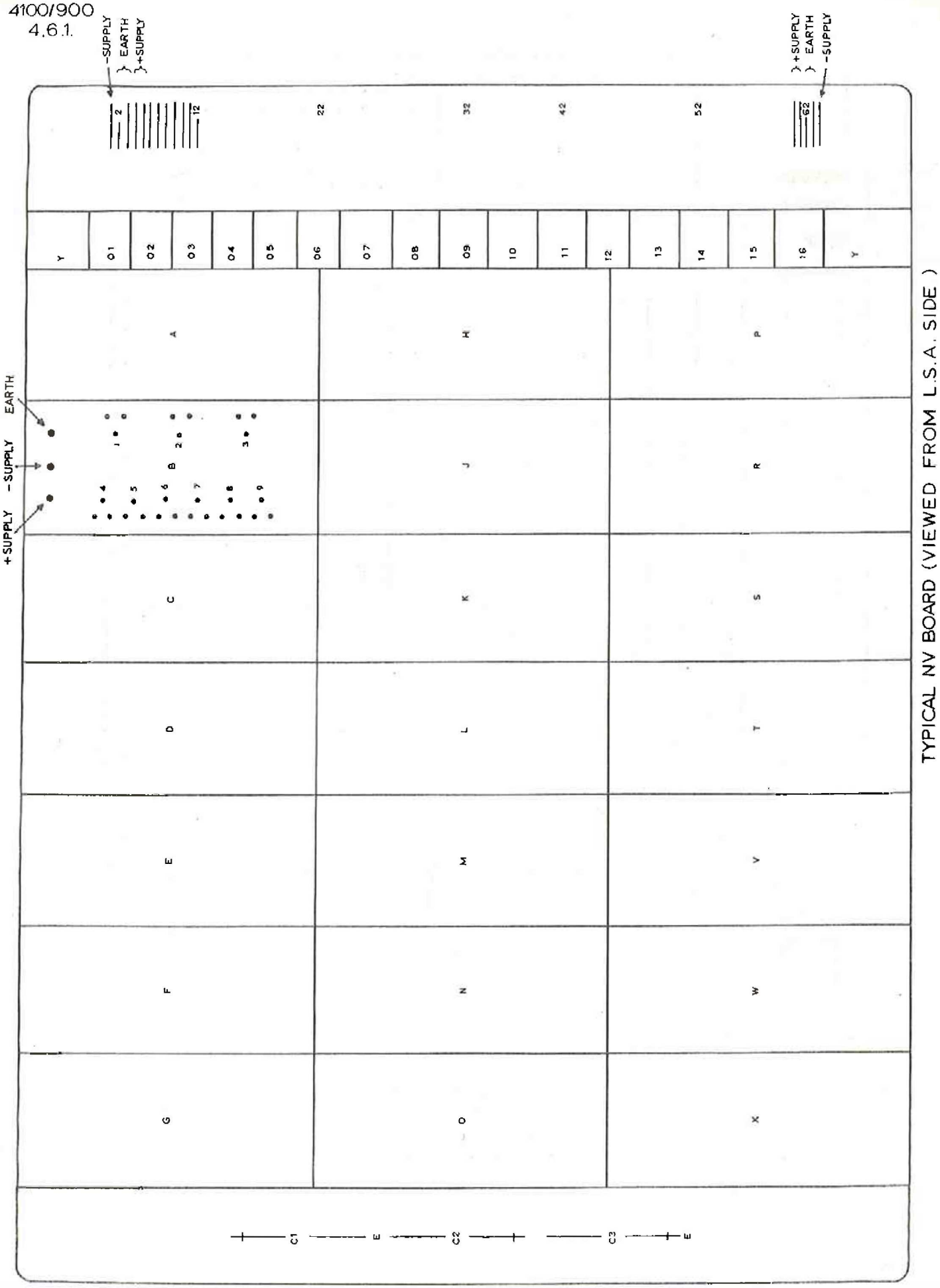
NOTES:

(1) PAD NUMBERS IN L.S.A AREAS ARE STANDARD

(2) PINS 33 TO 64 ARE ON OPPOSITE SIDE OF BOARD

TYPICAL DP BOARD (VIEWED FROM L.S.A. SIDE)

Figure 1 (ISSUE 3)

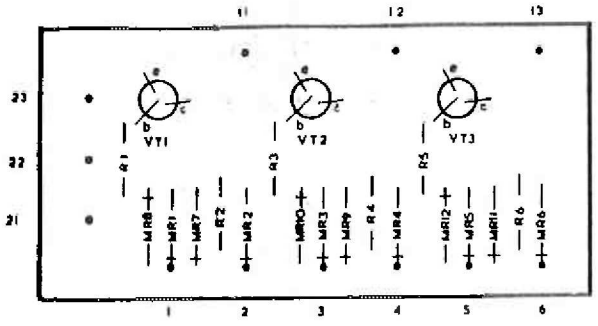


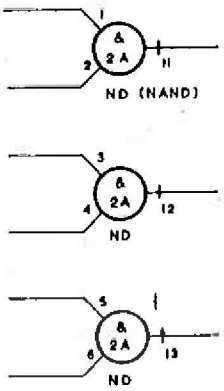
TYPICAL NV BOARD (VIEWED FROM L.S.A. SIDE)

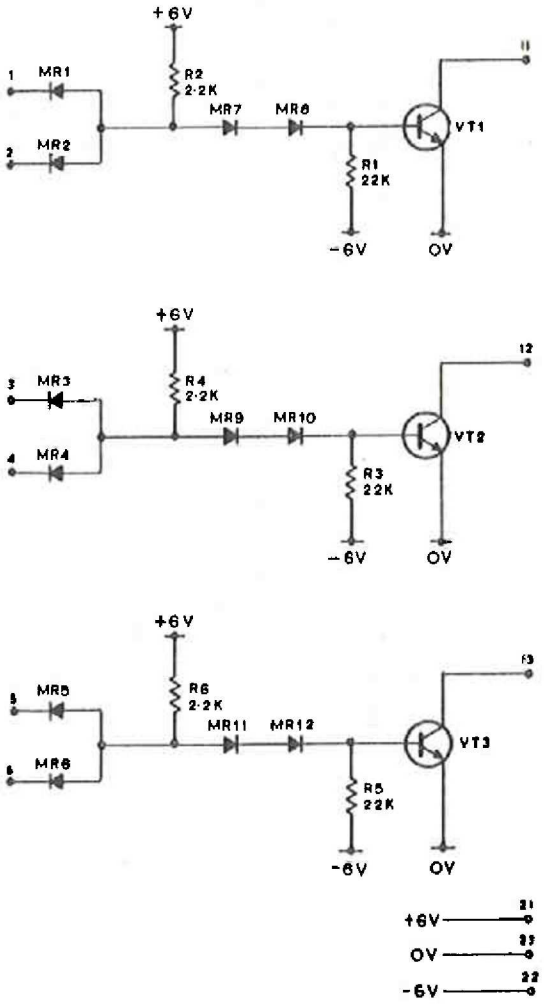
NOTE:
PAD NUMBERS IN L.S.A. AREAS ARE NON-STANDARD

Figure 2 (ISSUE 2)

TRANSISTOR	PURCH SPEC	CAT NO.
VT1–VT3	PS 218	11008



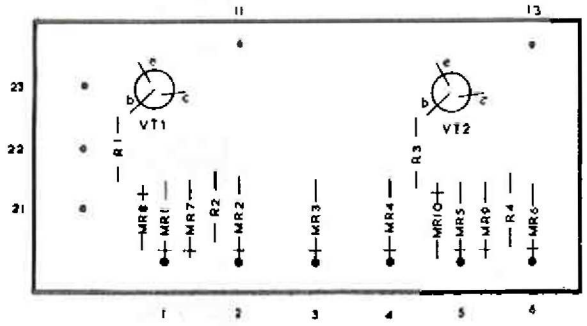


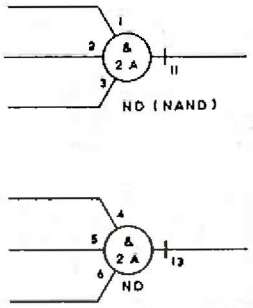


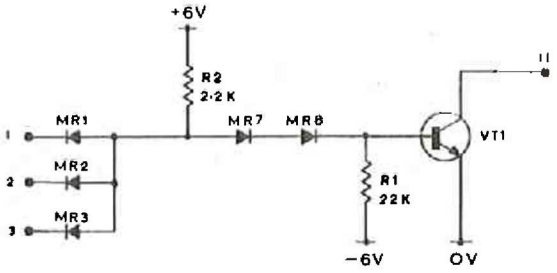
INPUT LOGIC LEVELS
'1' = > 2V
'0' = < 1V

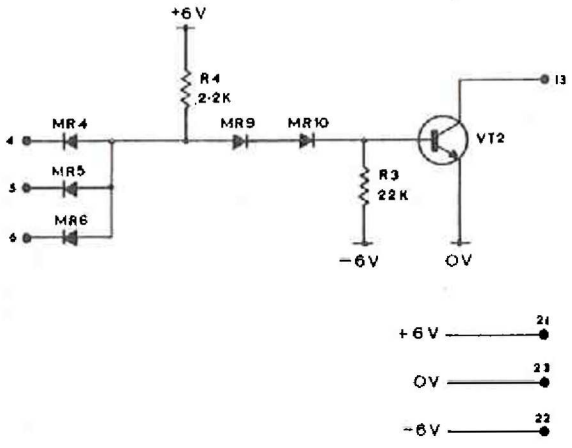
Figure 3 (ISSUE 2)

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1 VT2	PS 218	11008



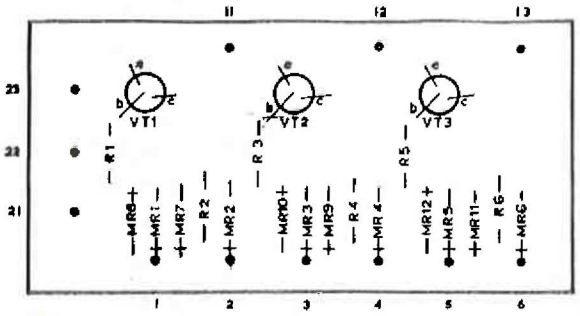


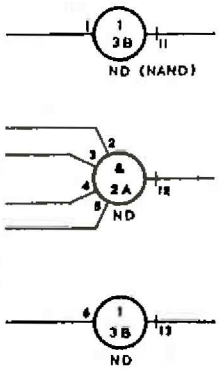


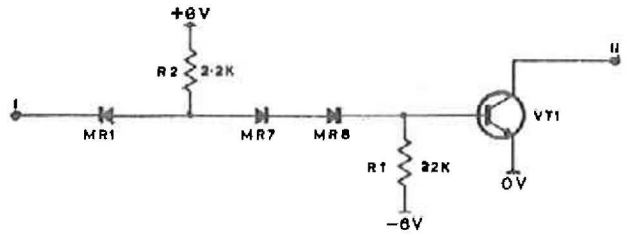


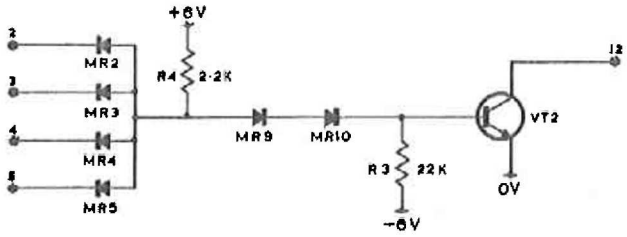
INPUT LOGIC LEVELS	
'1'	= > 2V
'0'	= < 1V

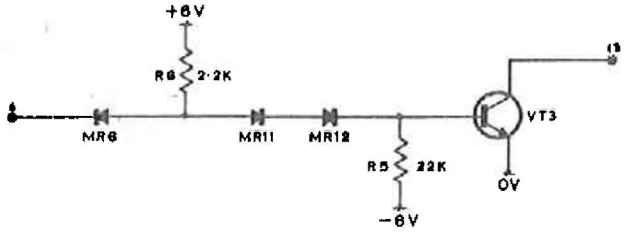
TRANSISTOR	PURCH. SPEC.	CAT. No
VT1–VT3	PS 218	11008

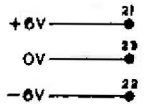






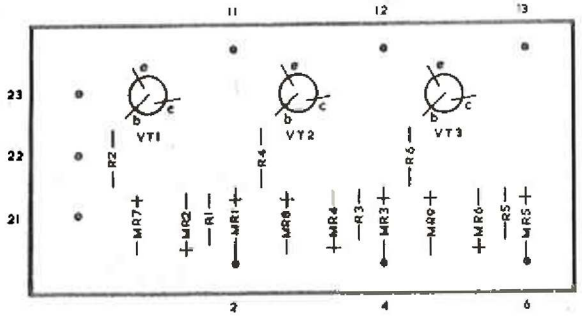


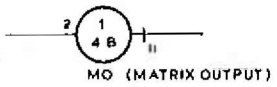


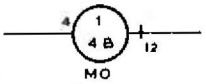


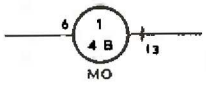
INPUT LOGIC LEVEL
'1' => 2V
'0' < 1V

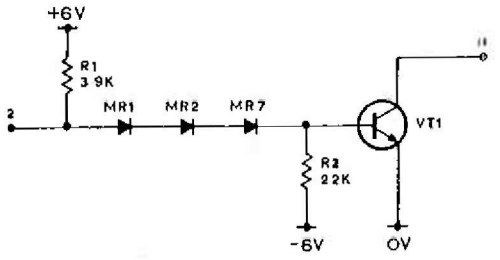
TRANSISTOR	PURCH. SPEC.	CAT NO.
VT1–VT3	PS 218	11008

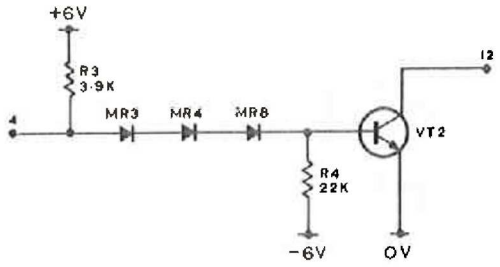


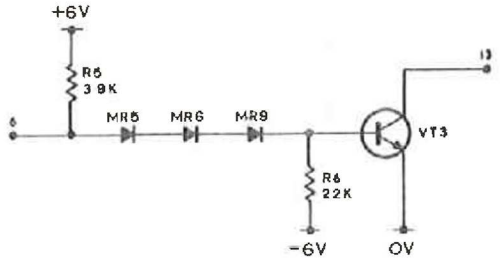


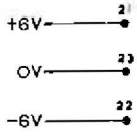








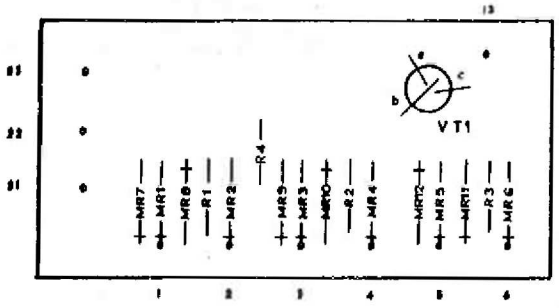


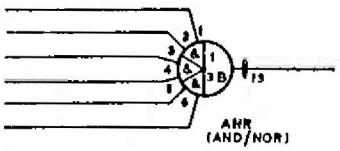


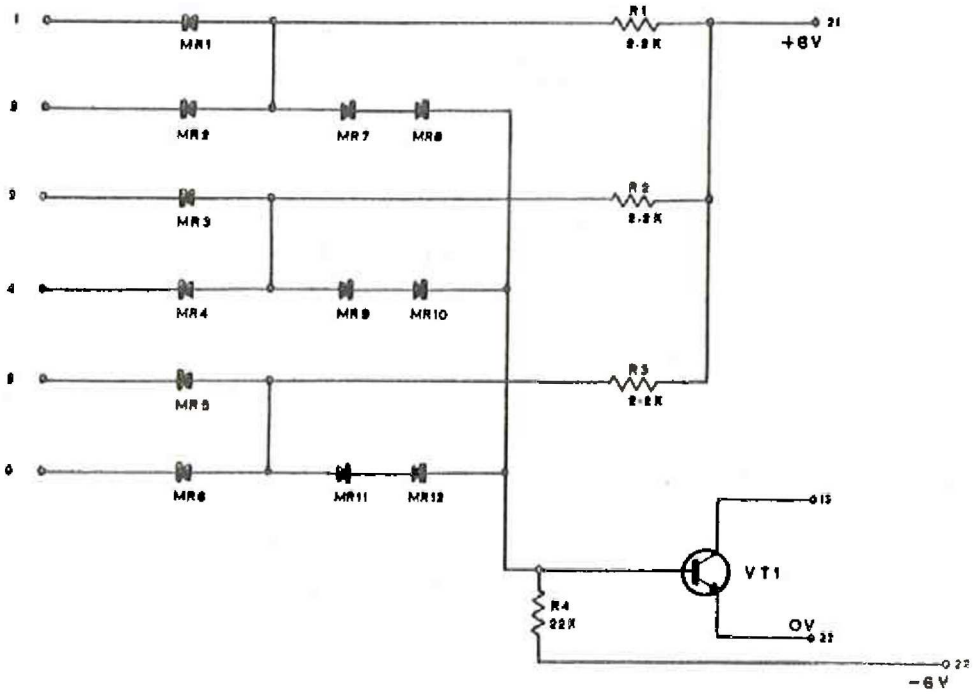
INPUT LOGIC LEVELS	
1	= > 3V
0	= < 1V

Figure 6 *(ISSUE 2)*

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1	PS 218	11006

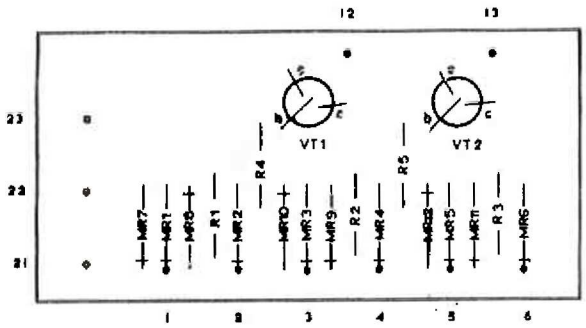


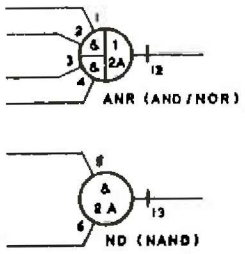


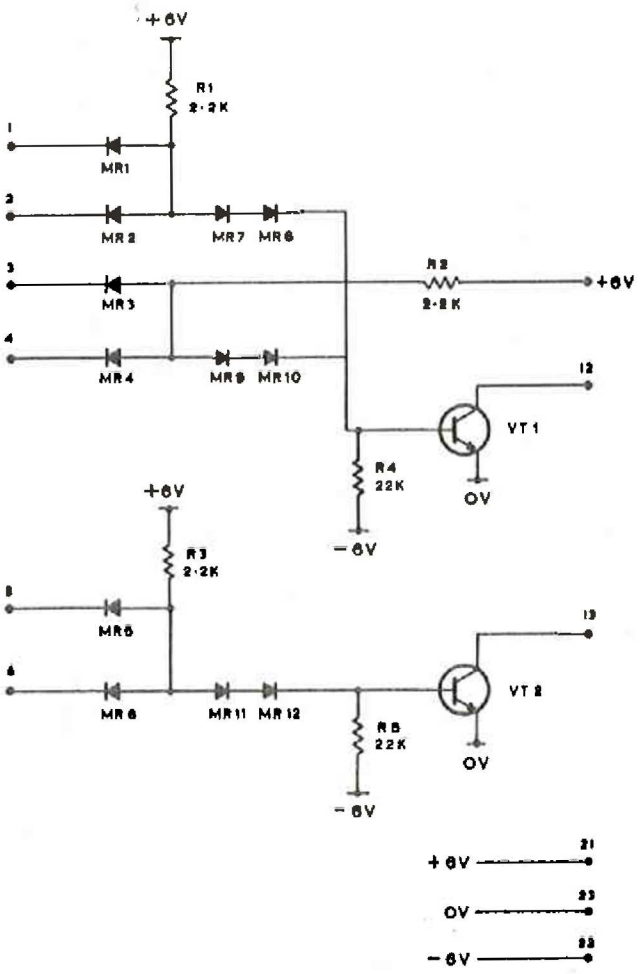


INPUT LOGIC LEVELS
'1' = > 2V.
'0' = < 1V

TRANSISTOR	PURCH SPEC	CAT NO.
VT1, VT2	PS 216	11008



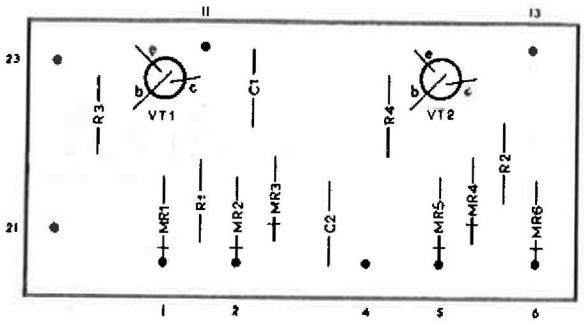


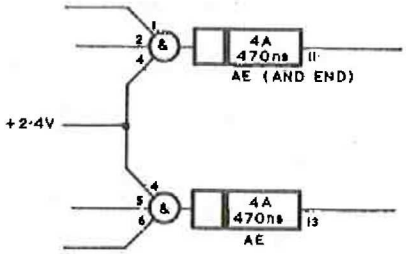


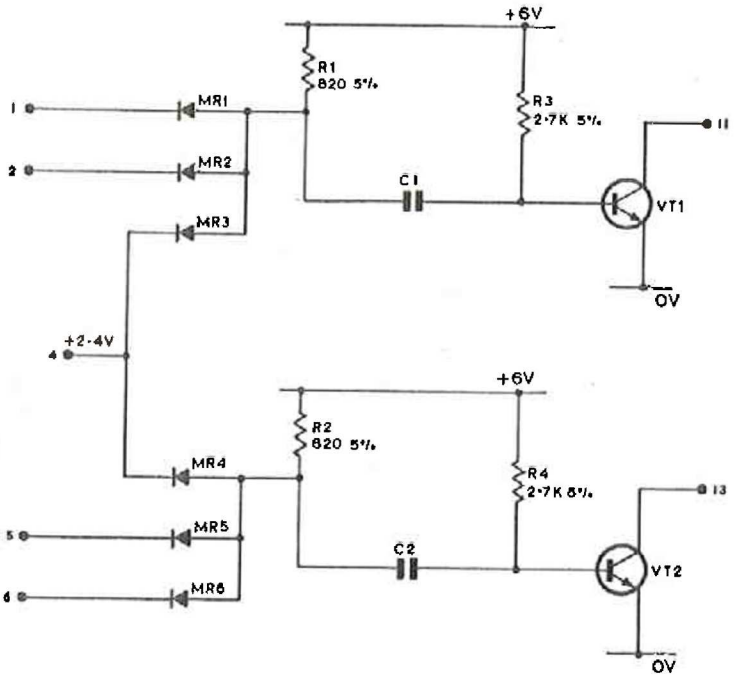
INPUT LOGIC LEVELS
'1' = >2V
'0' = <1V

Figure 8 (ISSUE 2)

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1, VT2	PS 218	11008







LSA No	C1 (pF)	C2 (pF)
07	100	100
13	330	330
137	220	220
138	470	470
34	100	330

NOTES:

(1) OUTPUT PULSE POSITIVE

(2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1' FOR GREATER THAN C/2 ns (WHERE C = CAPACITANCE IN pF)

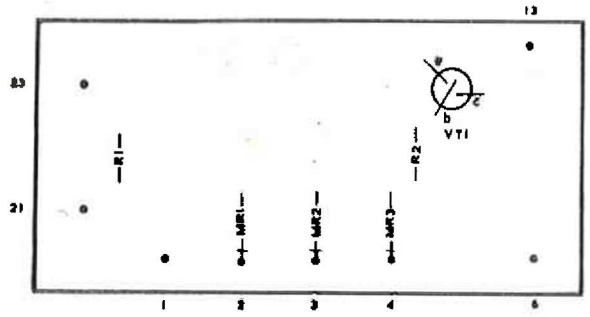
(3) PULSE WIDTH = Cns (WHERE C = CAPACITANCE IN pF)

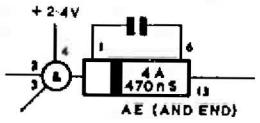
+6V ——● 21

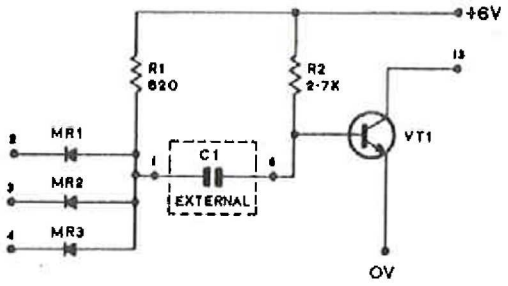
OV ——● 23

INPUT LOGIC LEVELS
'1' = >2V
'0' = <1V

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1	PS 218	11008







NOTES

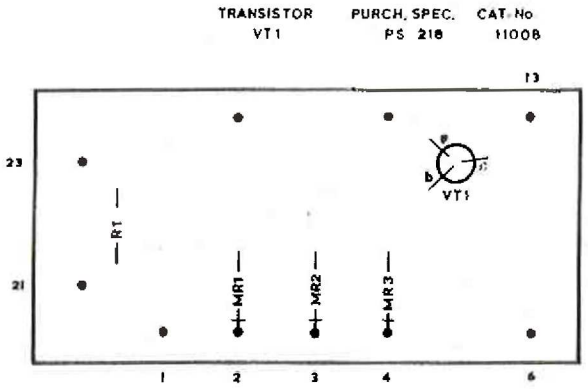
(1) OUTPUT PULSE POSITIVE.

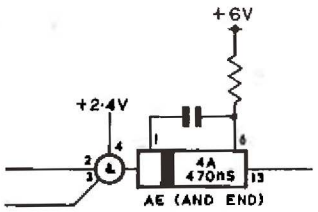
(2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/Ps HAVE BEEN '1' FOR > C/2 nS (WHERE C = CAPACITANCE IN pF).

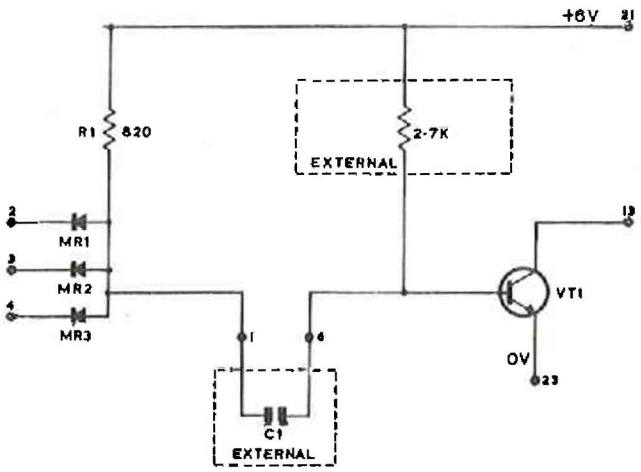
(3) PULSE WIDTH = (C nS) (WHERE C = CAPACITANCE IN pF)
C1 WILL BE AN EXTERNAL CAPACITOR.

INPUT LOGIC LEVELS
'1' = > 2V
'0' = < 1V

Figure 10 (ISSUE 2)







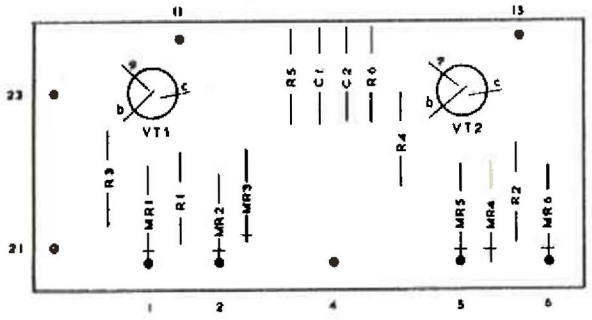
NOTES:
(1) OUTPUT PULSE POSITIVE.

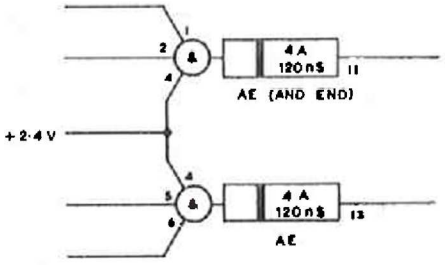
(2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P's HAVE BEEN '1' FOR > C/2 nS

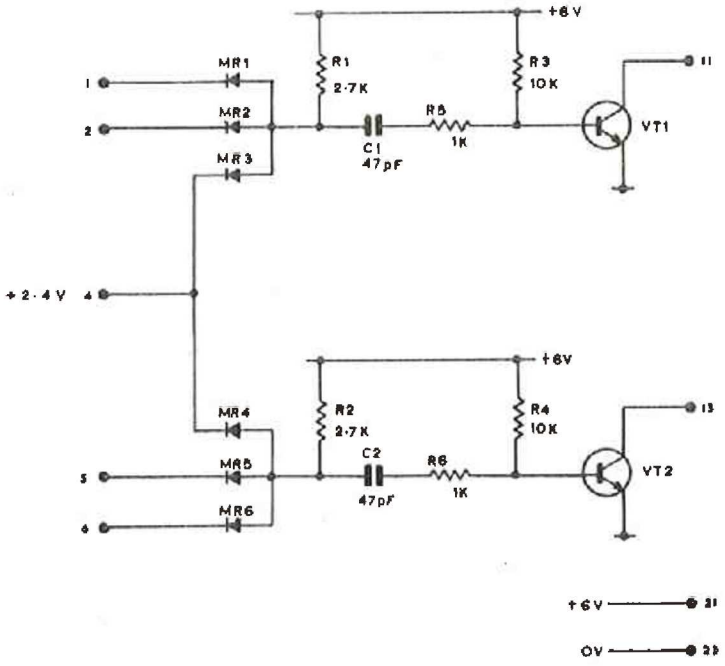
(3) PULSE WIDTH = C nS (WHERE C = CAPACITANCE IN pF.)

INPUT LOGIC LEVELS
'1' = > 2V
'0' = < 1V

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1 VT2	PS 216	11008







NOTES :-

(1) OUTPUT PULSE POSITIVE

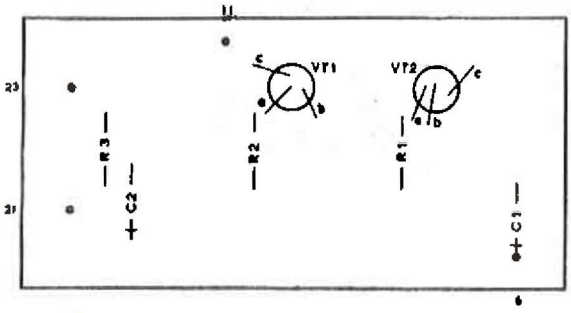
(2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1' FOR GREATER THAN 60 nS.

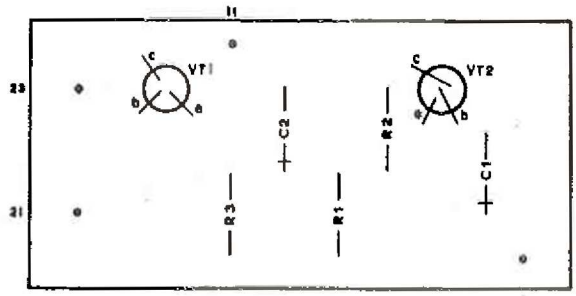
(3) PULSE WIDTH = 120 nS ± 20%

INPUT LOGIC LEVELS		
'1'	=	> 2V
'0'	=	< 1V

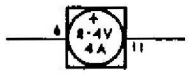
Figure 12 *(ISSUE 2)*

TRANSISTOR	CAT. NO.
VT1, VT2	11740

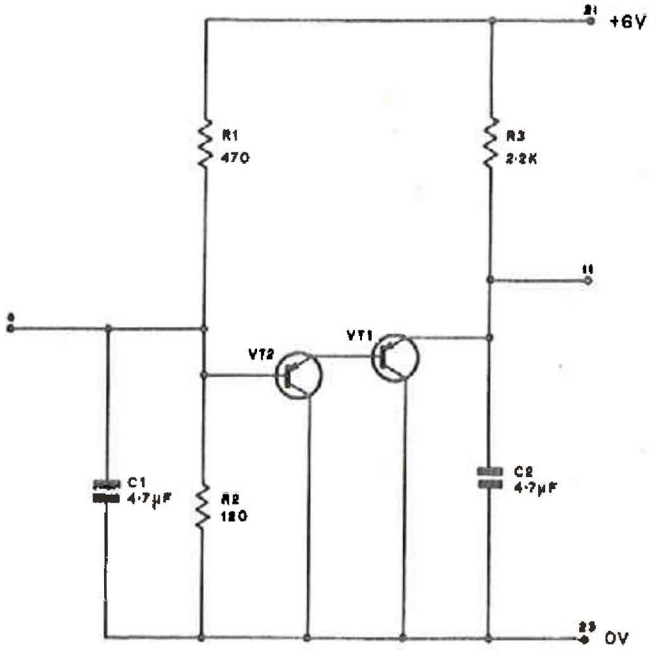




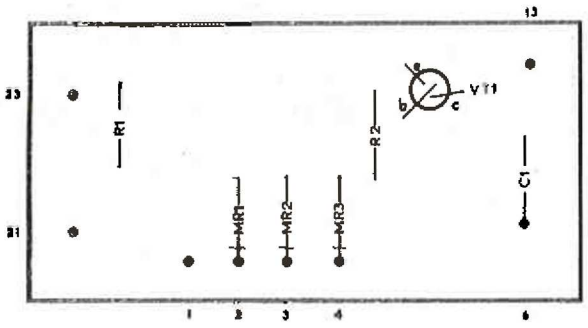
Alternative Layout.

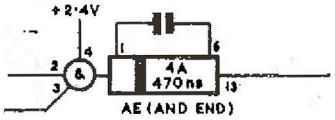


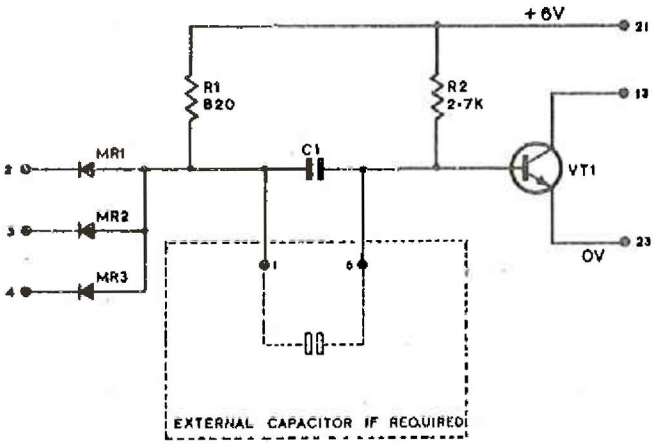
VR (VOLTAGE REFERENCE)



TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1	PS 218	11008







LSA Nº	C1	PULSE WIDTH
09	470pF	470ns
14	680pF	680ns
130	·22μF	220μs
131	2·2μF	2·2ms

NOTES:

(1) OUTPUT PULSE POSITIVE

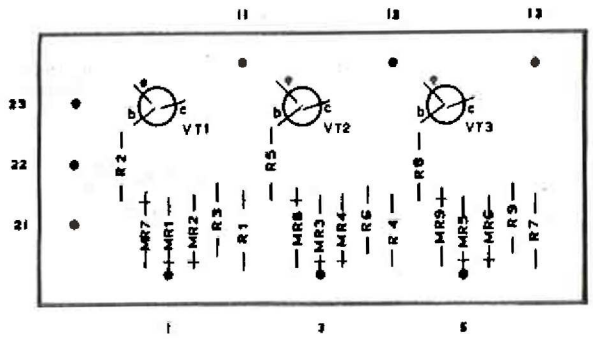
(2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1' FOR >C/2ns. (WHERE C = CAPACITANCE IN pF)

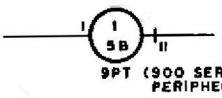
(3) PULSE WIDTH = Cns (WHERE C = CAPACITANCE IN pF)

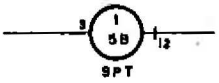
(4) C1 MAY BE INCREASED BY EXTERNAL CAPACITOR

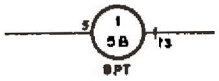
INPUT LOGIC LEVELS
'1' = >2V
'0' = <1V

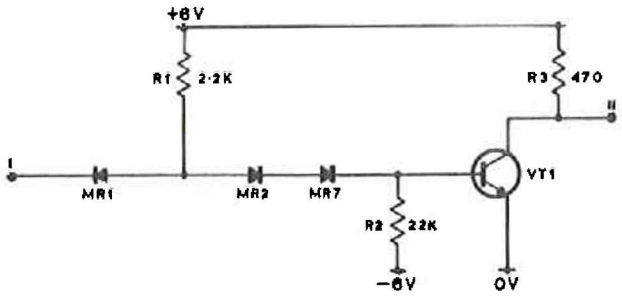
TRANSISTOR	PURCH. SPEC.	CAT. No.
VT1–VT3	PS 218	11008

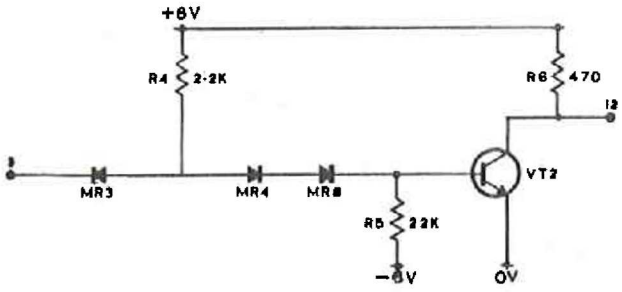


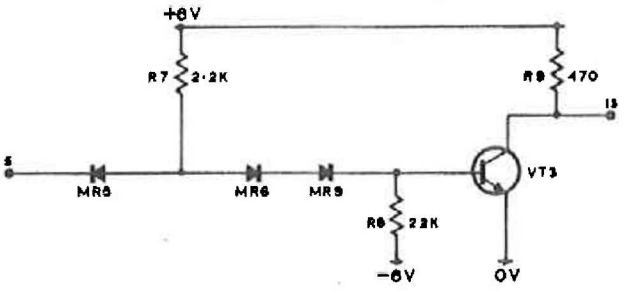


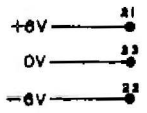






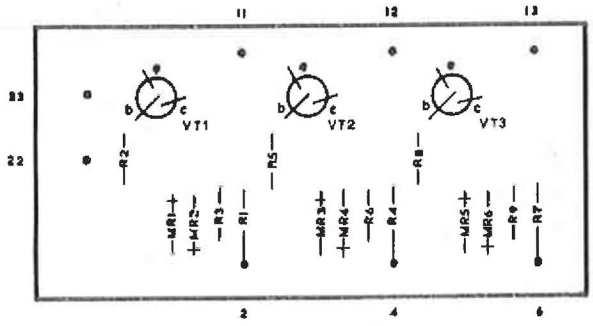


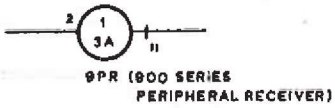


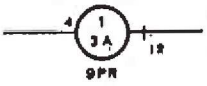


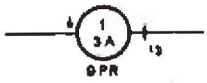
INPUT LOGIC LEVELS
'1' > 2V
'0' < 1V

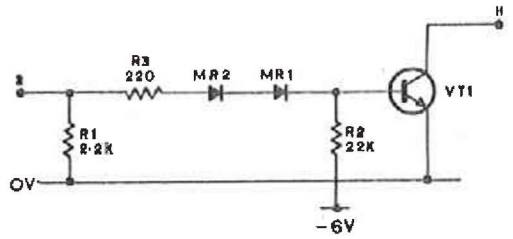
TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1—VT3	PS 218	11008

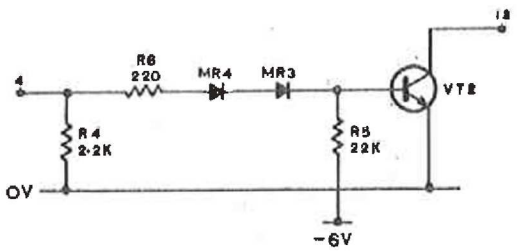


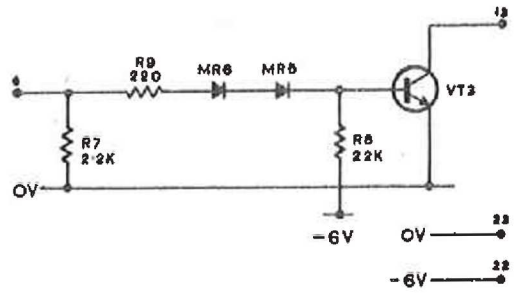






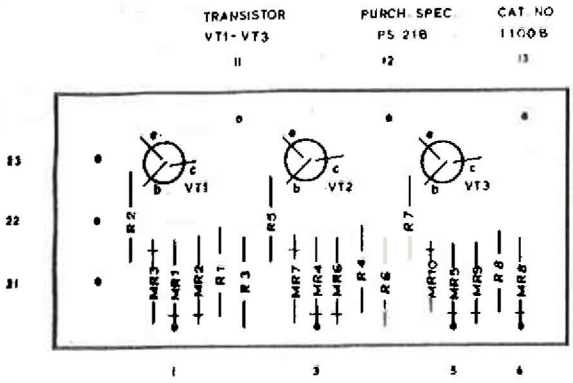


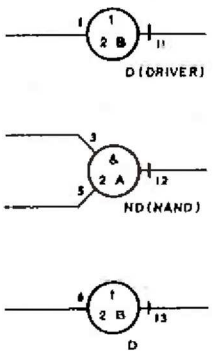


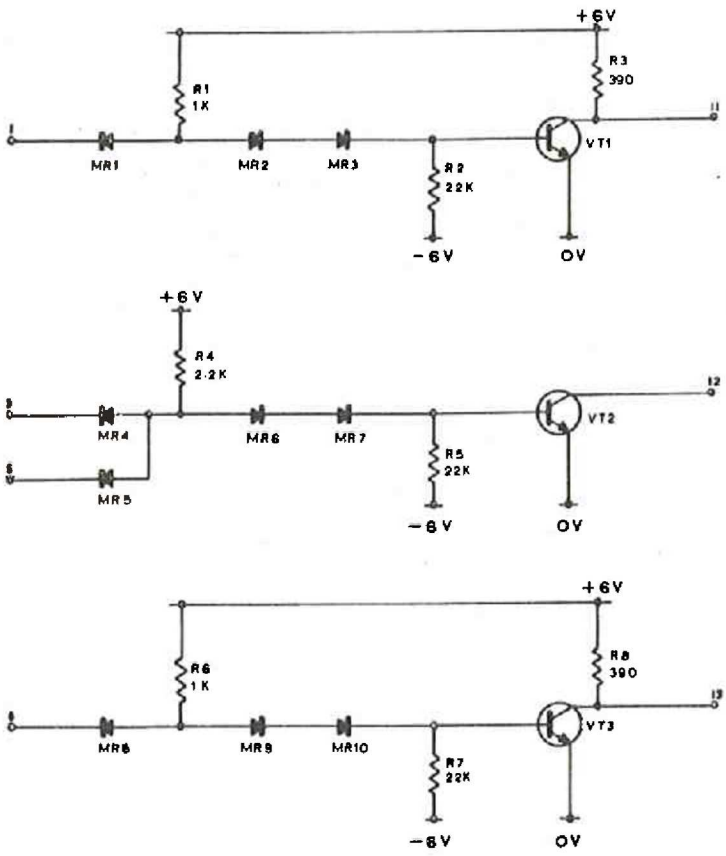


INPUT LOGIC LEVELS
'1' = > 3 V
'0' = < 1 V

Figure 16 *(ISSUE 2.)*



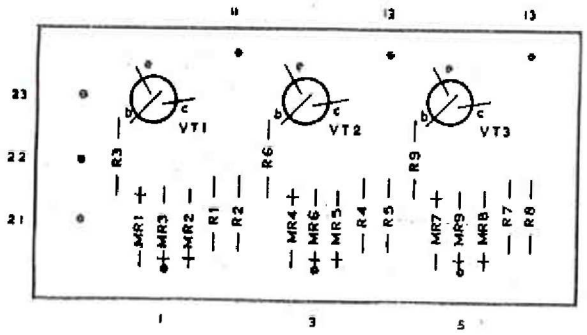


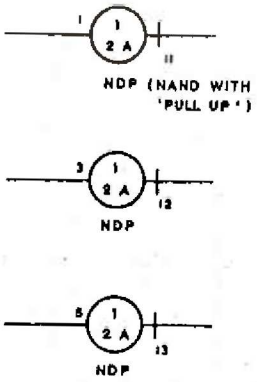


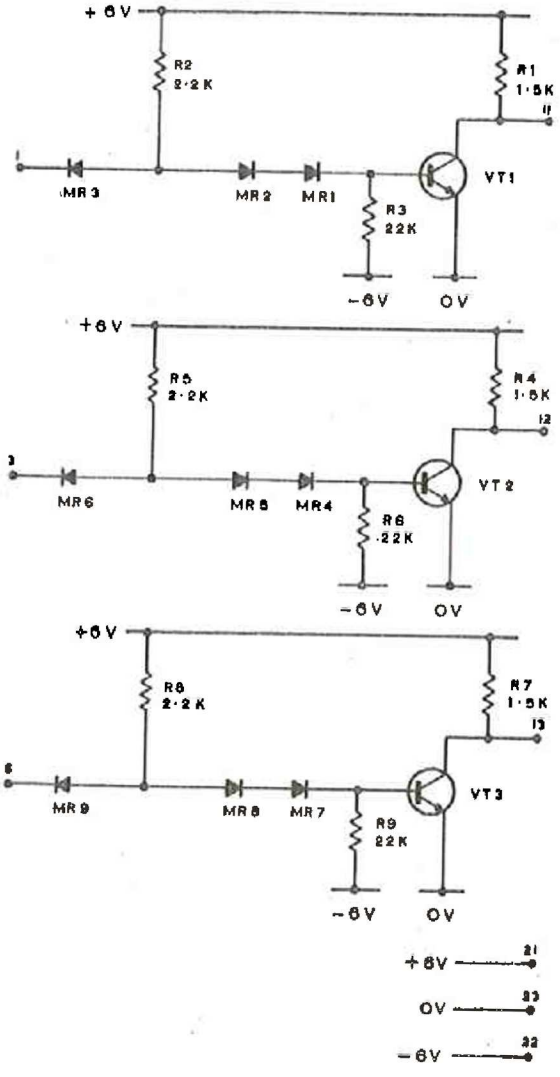
INPUT LOGIC LEVELS
'1' = > 2 V
'0' = < 1 V

Figure 17 (ISSUE 2)

TRANSISTOR	PURCH SPEC	CAT NO
VT1- VT3	PS 218	11008



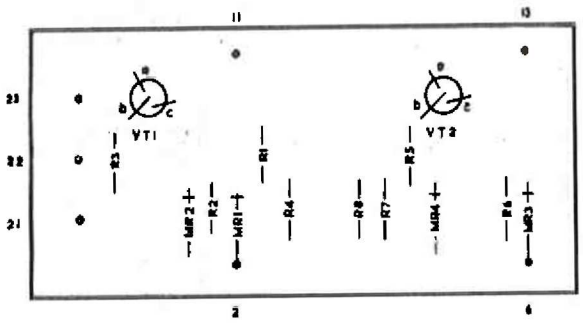


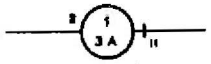


INPUT LOGIC LEVELS		
'1'	=	> 2 V
'0'	=	< 1 V

Figure 18 (ISSUE 2)

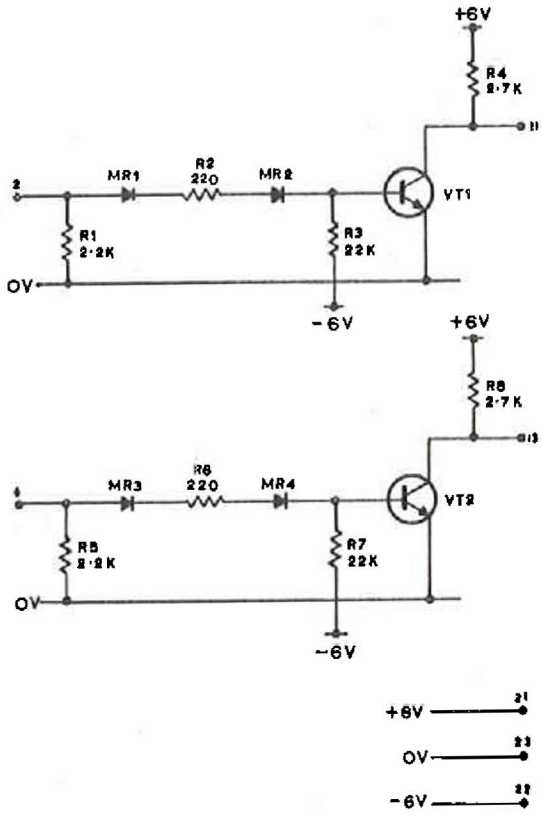
TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1, VT2	PS218	11008





PRP (PERIPHERAL RECEIVER WITH PULL UP)

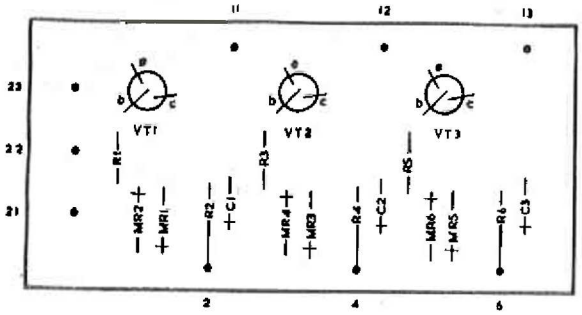
PRP

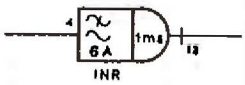


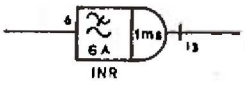
INPUT LOGIC LEVELS
'1' = > 3V
'0' = < 1V

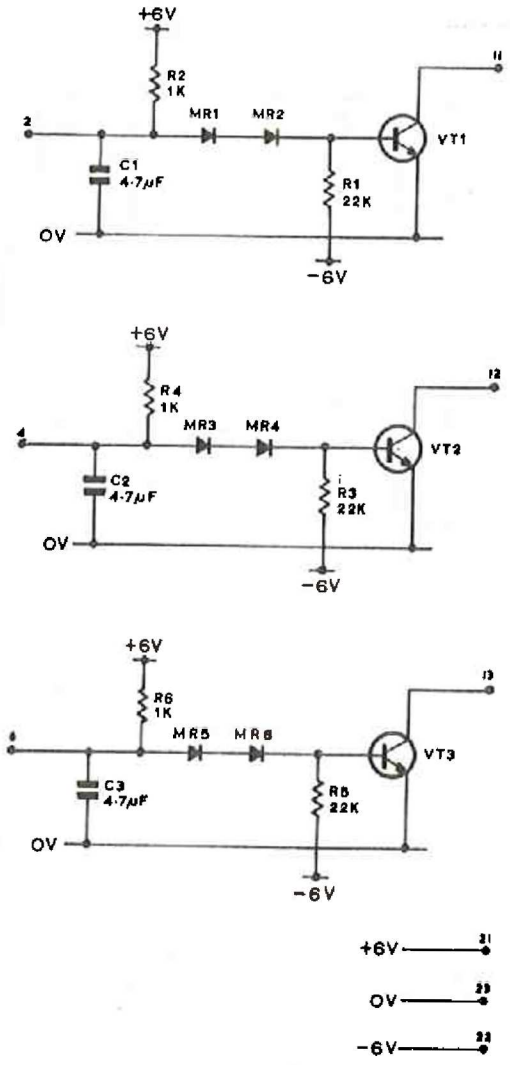
Figure 19 (ISSUE 2)

TRANSISTOR	PURCH.SPEC.	CAT. NO.
VT1—VT3	PS 218	11008





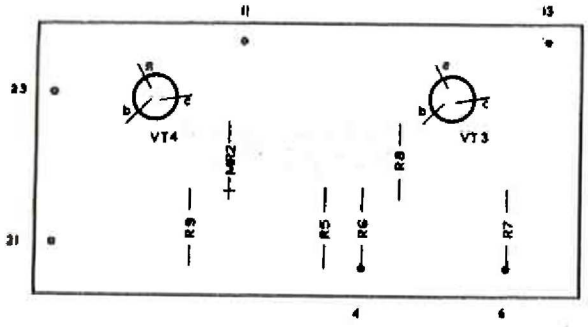




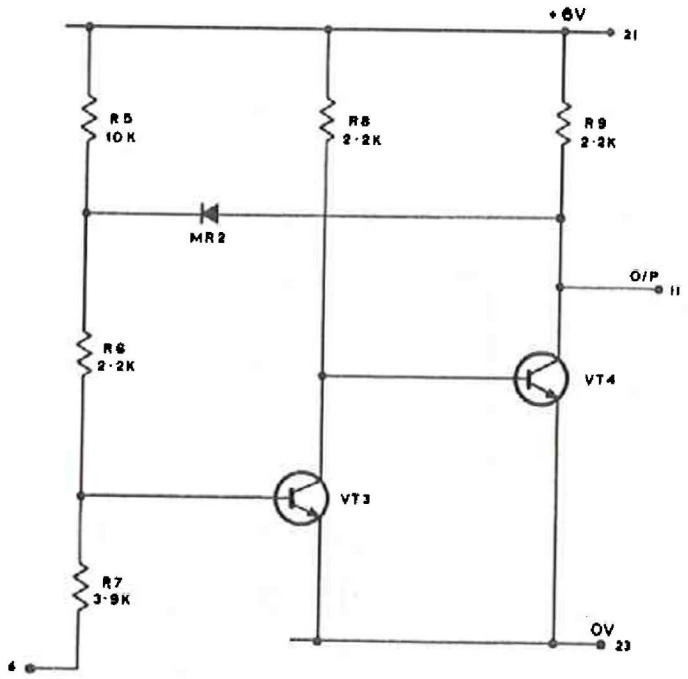
INPUT LOGIC LEVELS
'1' = > 2V
'0' = < 1V

Figure 20 *(ISSUE 2.)*

TRANSISTOR	PURCHASE SPEC.	CAT. NO.
VT3 VT4	PS218	11008

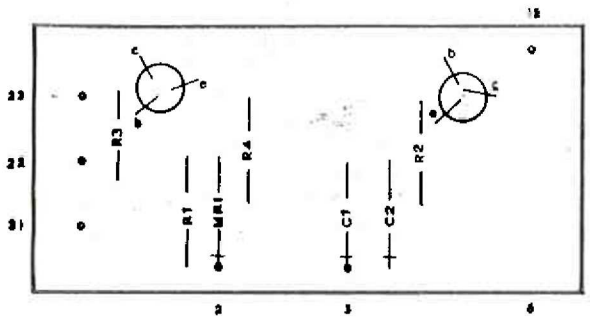


NOTE :-
L.S.A. 19 ALWAYS FOLLOWS L.S.A. 20, 21, 24 OR 25. THE SYMBOL SHOWN IS A COMBINED SYMBOL FOR THE 2 ELEMENTS.

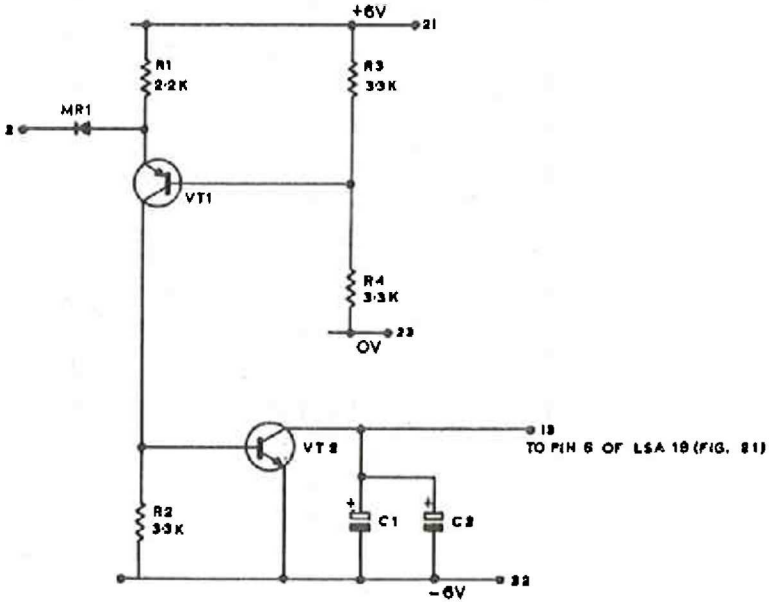


INPUT THRESHOLD LEVEL
(AT 25°C) = -0·4v ±10 %

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1	—	14581
VT2	PS 218	11008



L.S.A. 19 ALWAYS FOLLOWS L.S.A. 20, 24 OR 25 . SEE FIG. 21 FOR COMBINED SYMBOL.



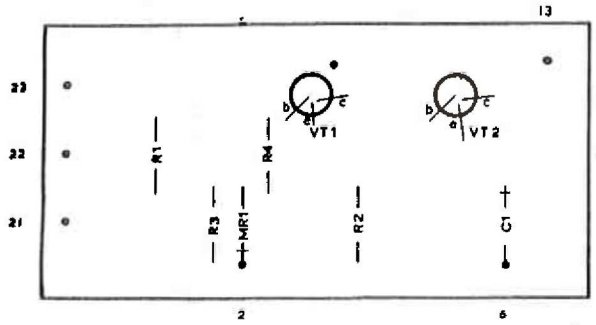
L.S.A. No.	C1 μF	C2 μF	DELAY mS
20	4·7	4·7	94
24	2·2	1·0	32
25	2·2	0·47	26·7

NOTE 1
DELAY Δ 10 mS PER μF (WHERE μF IS CAPACITANCE OF C1 & C2)

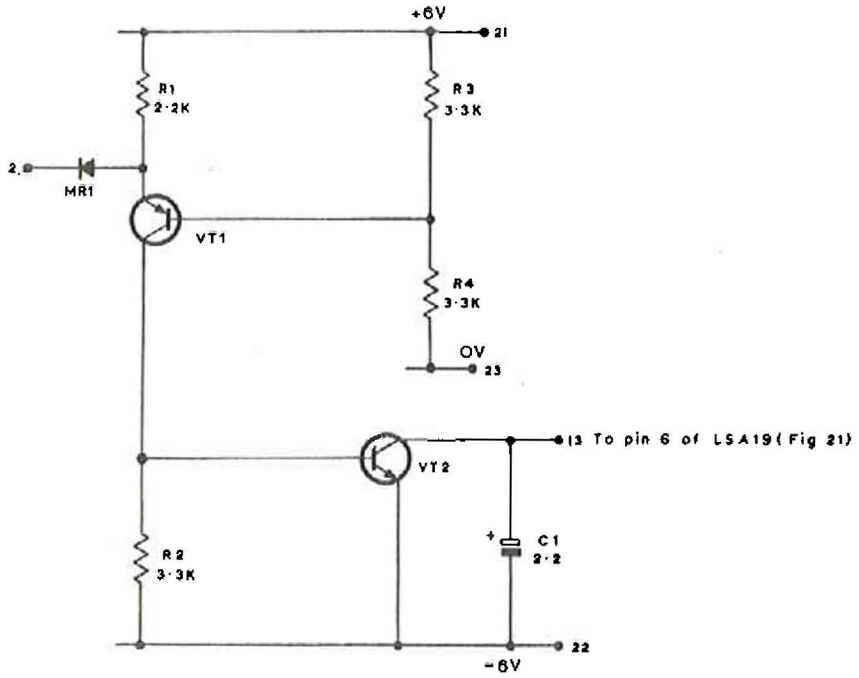
INPUT LOGIC LEVELS
'1' = > 3V
'0' = < 1V

Figure 22 (ISSUE 2)

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1	—	14581
VT2	PS218	11008



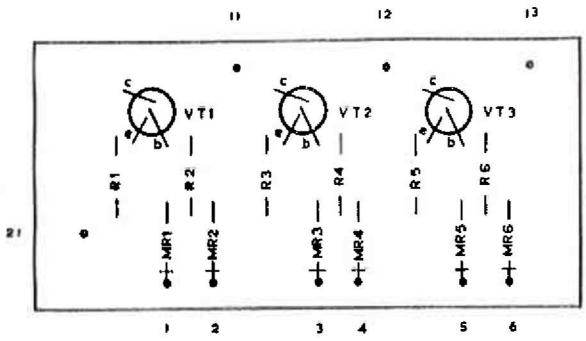
L.S.A.19 ALWAYS FOLLOWS
L.S.A. 21 SEE FIGURE. 21
FOR COMBINED SYMBOL.

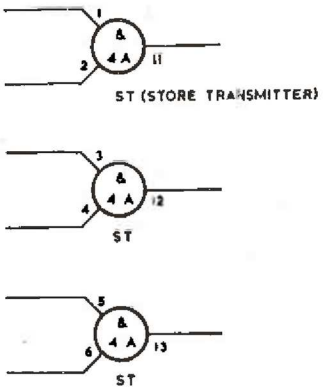


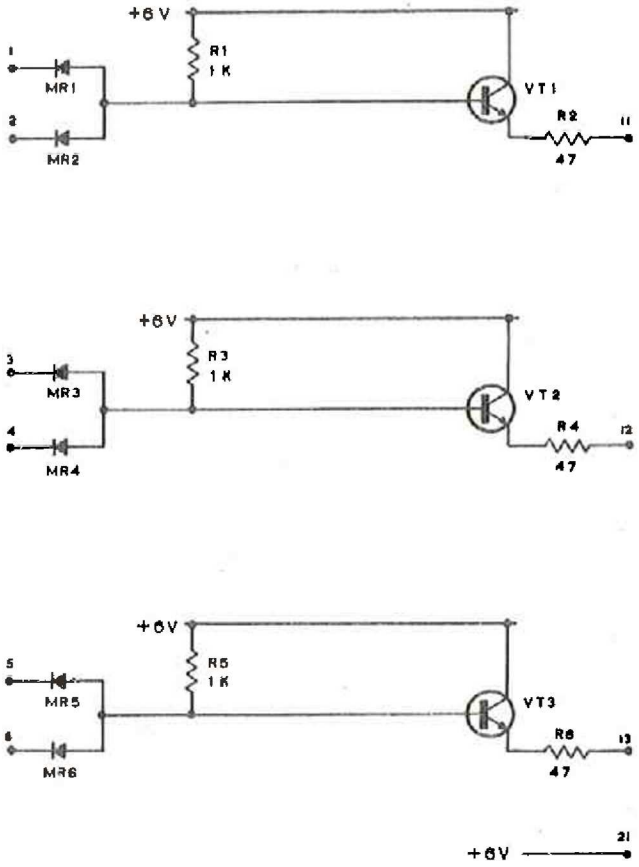
NOTE:
1. DELAY $\triangleq$ 10mS PER μF
(WHERE μF IS CAPACITANCE
OF C1) $\triangleq$ 22mS.

INPUT LOGIC LEVELS		
'1'	=	> 3V
'0'	=	< 1V

TRANSISTOR	PURCH SPEC	CAT NO.
VT1 – VT3	PS 218	11008

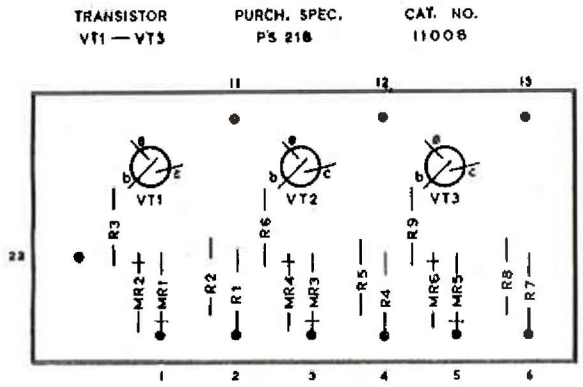


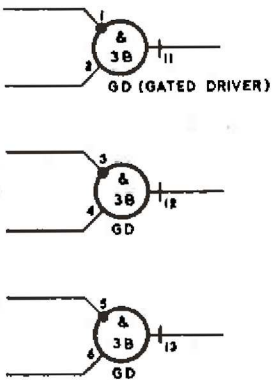




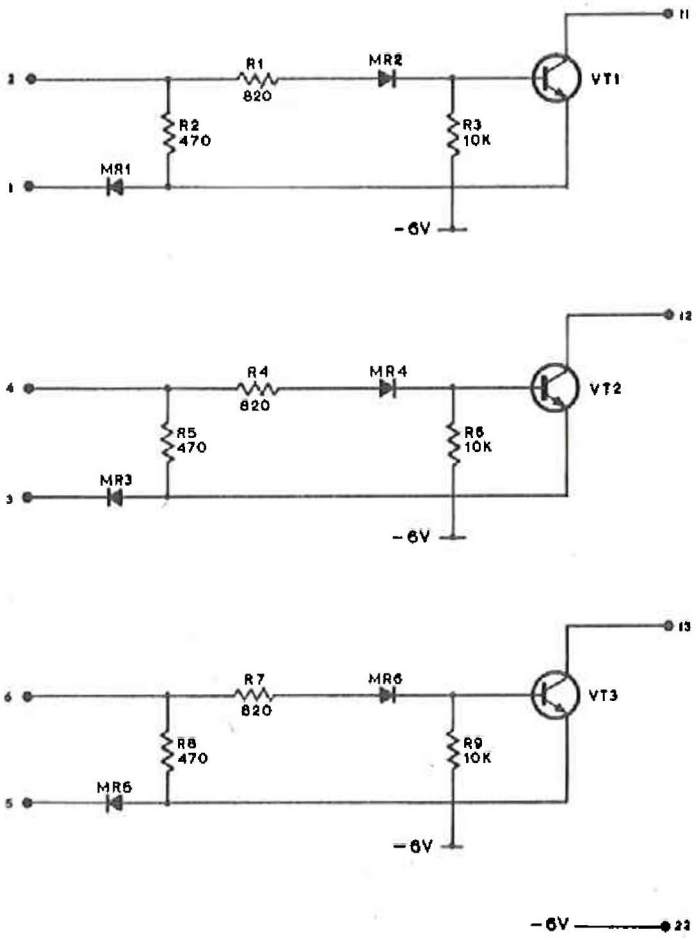
INPUT LOGIC LEVELS
(1) O/P FOLLOWS I/P OVER RANGE 0V TO 4·7V
(2) WHEN DRIVING A RECEIVER THE LOGIC LEVELS ARE :-
'1' = >3V
'0' = <1V

Figure 24 *(ISSUE 2)*



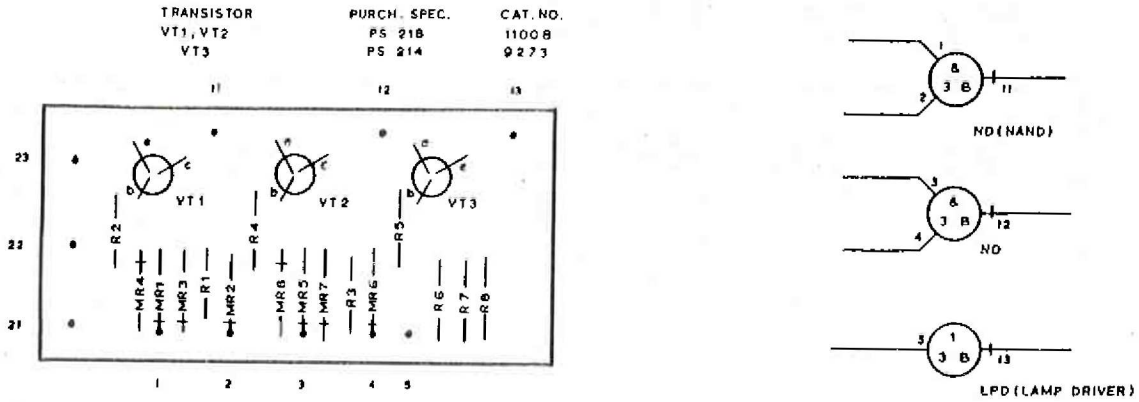


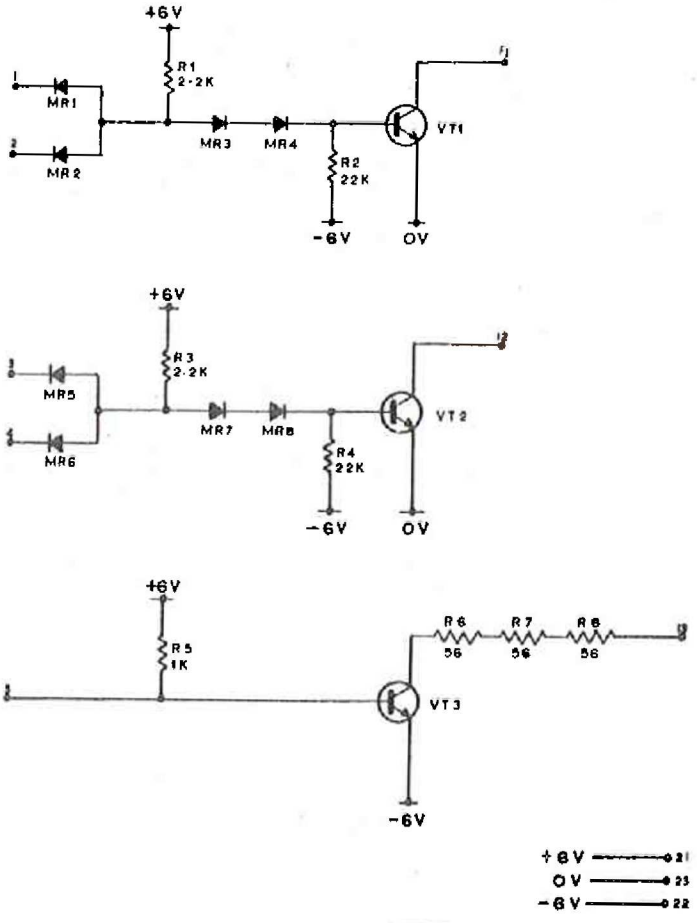
* SEE ERRATA PAGE 1.



INPUT LOGIC LEVELS
'1' = > 3V
'0' = < 1V

Figure 25 (ISSUE 2)

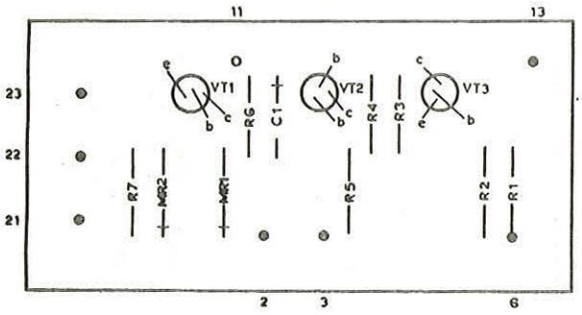


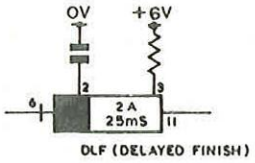


INPUT LOGIC LEVELS	
NAND GATES	'1' = > 2 V '0' = < 1 V
LAMP DRIVER	'1' = > 0,45V '0' = < 0,25V

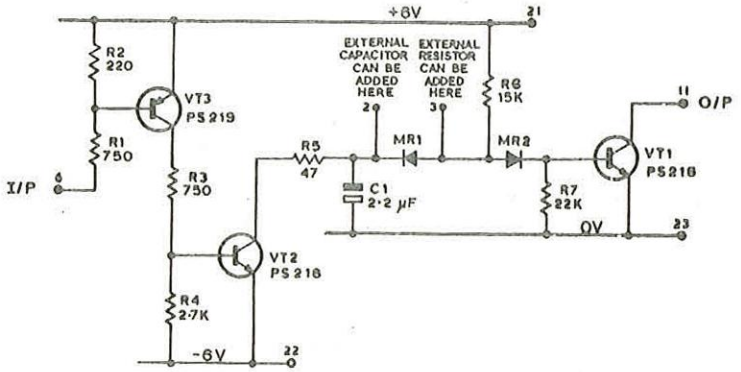
Figure 26 (ISSUE 2)

TRANSISTOR	PURCH. SPEC.	CAT. No.
VT1, VT2	PS 218	11008
VT3	PS 219	11009

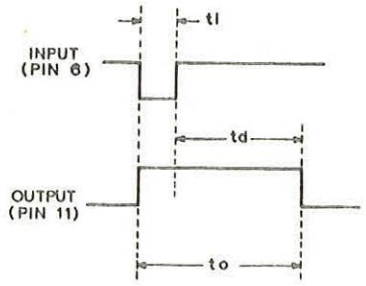




DLF (DELAYED FINISH)



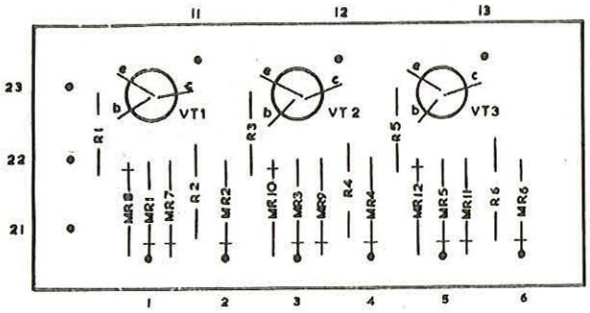
NOTE:
1. SHUNT C1 TO MAKE O/P > 25mS.
2. SHUNT R6 TO MAKE O/P < 25mS.

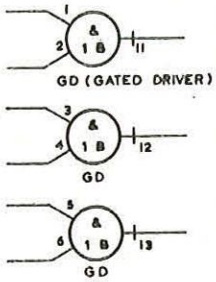


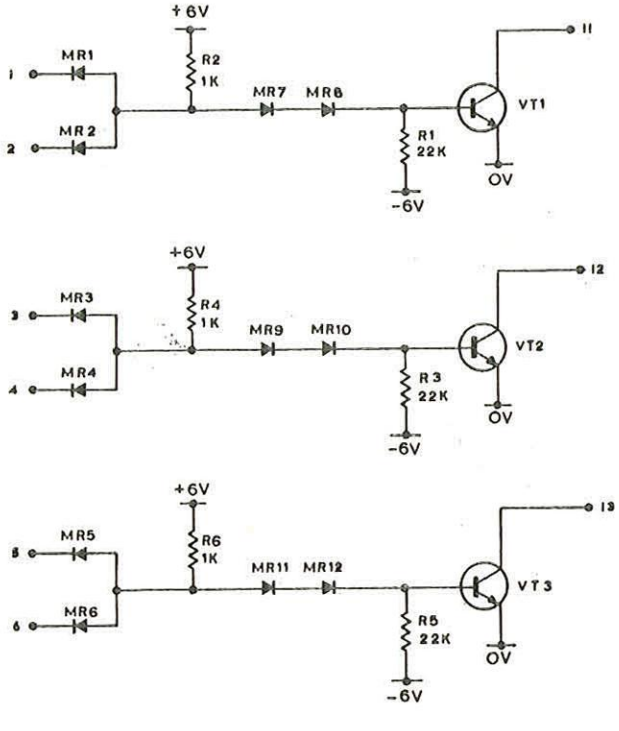
td NOMINAL = 25mS
td RANGE = 1m - 5 Secs.
td TOLERANCE = ± 30%

INPUT LOGIC LEVELS
'1' = > 5·4V
'0' = < 1V

TRANSISTOR	PURCH SPEC.	CAT. NO.
VT1 – VT3	PS 218	11008



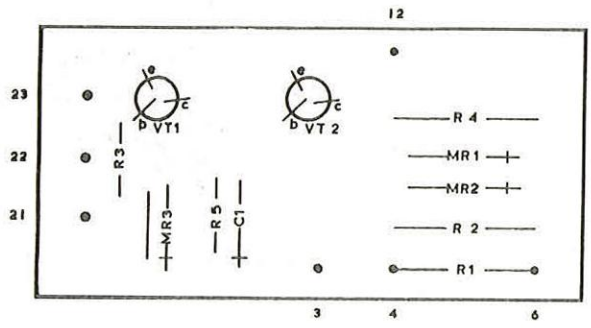


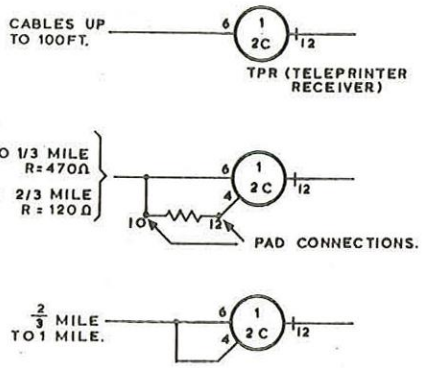


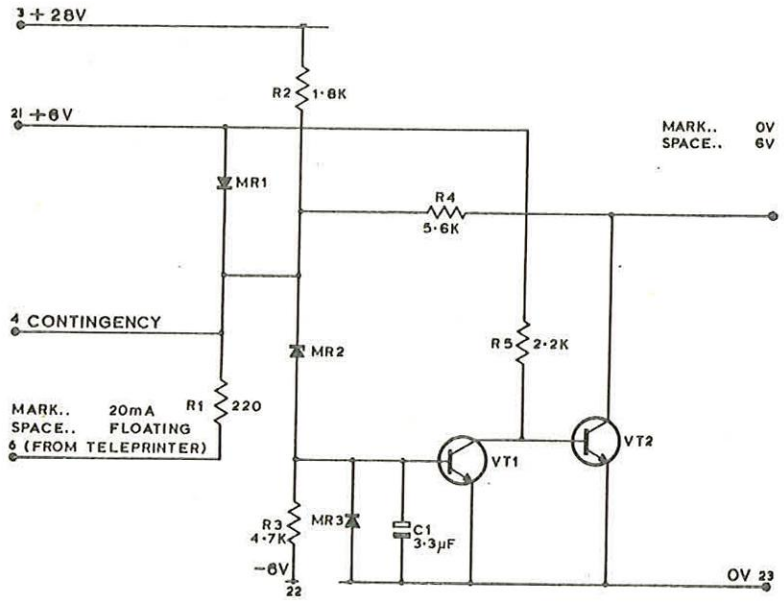
INPUT LOGIC LEVELS
'1' = > 2V
'0' = < 1V

Figure 28 (ISSUE 2)

TRANSISTOR	PURCH. SPEC.	CAT. No.
VT1, VT2	PS 218	11008



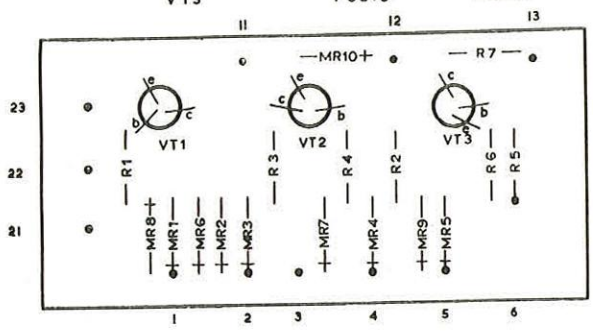


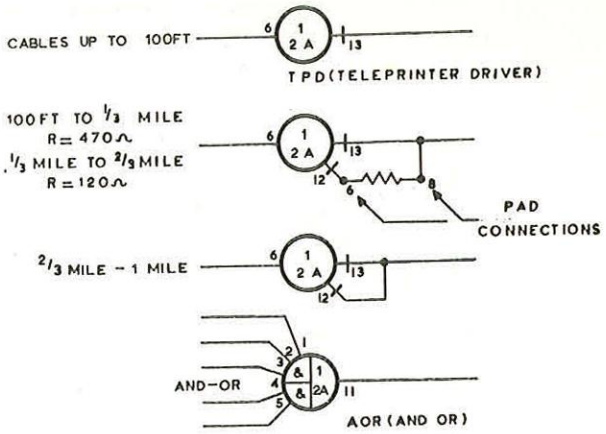


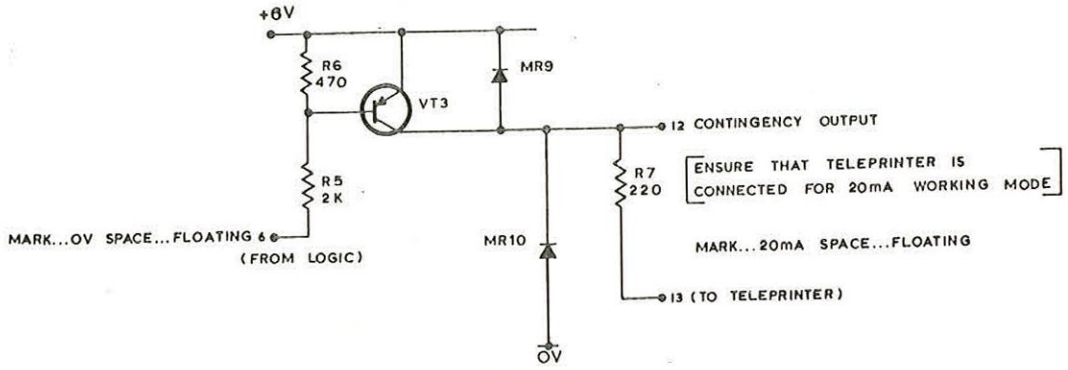
NOTE:
THE ELEMENT IS CONSIDERED TO INVERT BECAUSE THE MARK CURRENT IS TAKEN TO REPRESENT A LOGIC "1," EVEN THOUGH THE POTENTIAL AT PIN 6 FALLS UNDER MARK CONDITIONS.

INPUT LOGIC LEVELS
0 = > 5V
1 = < 0·4V (ASSUMING NO EXTERNAL R AT PIN 4)

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1, VT2	PS218	11008
VT3	PS219	11009

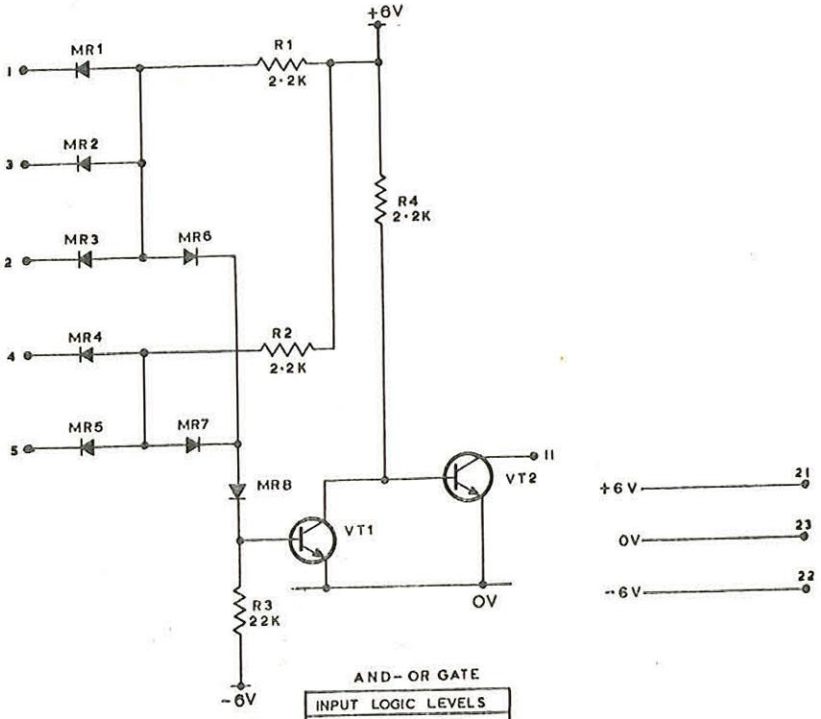






TELEPRINTER DRIVER

INPUT LOGIC LEVELS
'1' = > 4V
'0' = < 1 V

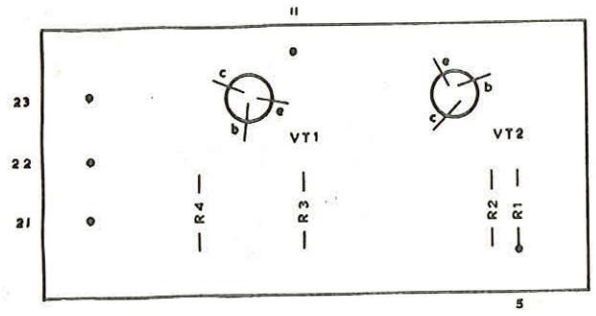


AND-OR GATE

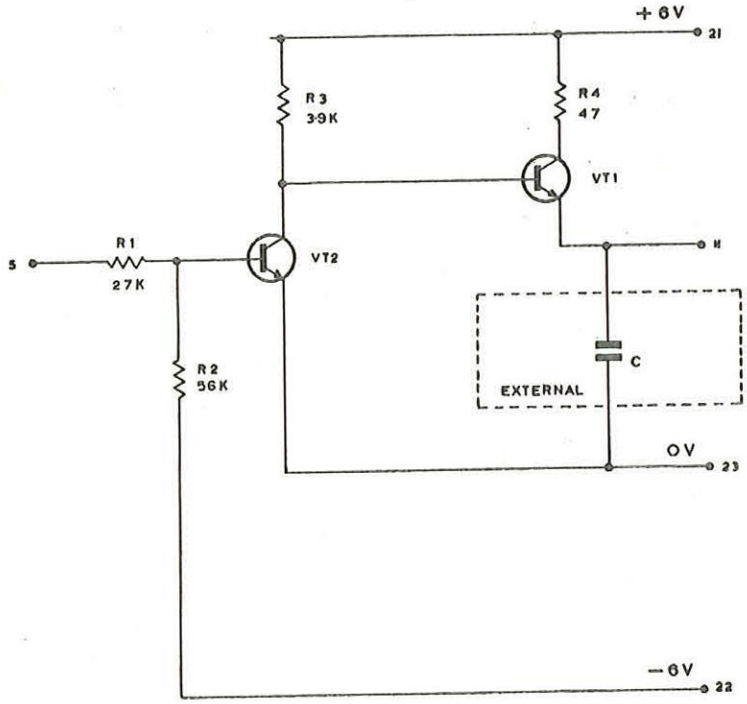
INPUT LOGIC LEVELS
'1' = > 2V
'0' = < 1V

Figure 30 (ISSUE 2)

TRANSISTOR	PURCH SPEC	CAT NO.
VT1, VT2	PS 212	8843



SEE FIGURE 32 FOR SYMBOL



NOTES:

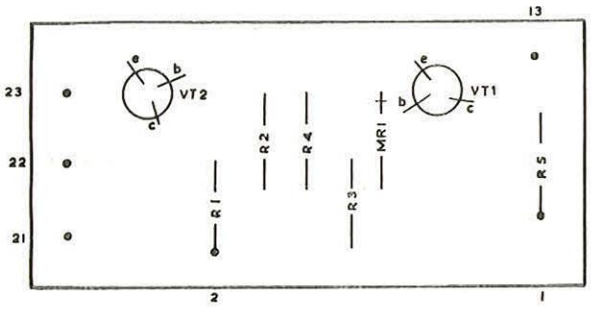
(1) INPUT VOLTAGE LEVELS ARE '1' = +12V ±3V; '0' = 0V ±3V

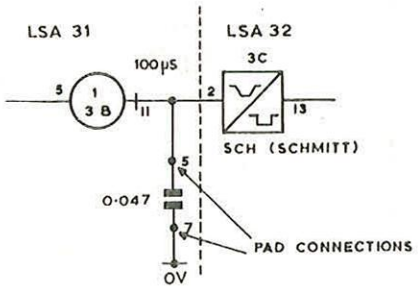
(2) C. IS CONNECTED EXTERNALLY WHEN USED IN CONJUNCTION WITH A RESISTOR ON L.S.A. 32

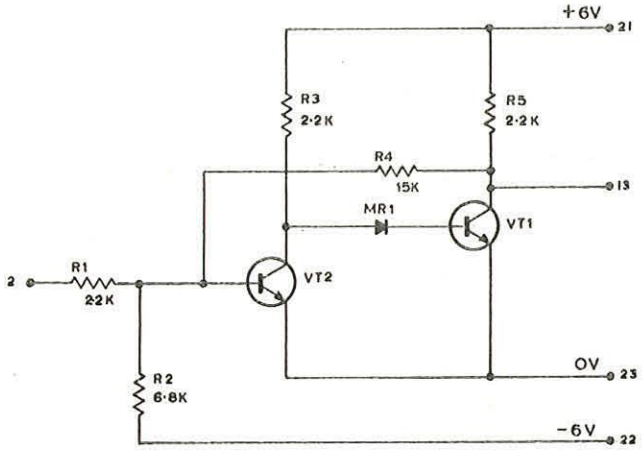
(3) C. = 0·047μF FOR A DELAY OF 100·μS.

Figure 31 (ISSUE 3)

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1, VT2	PS 212	8843

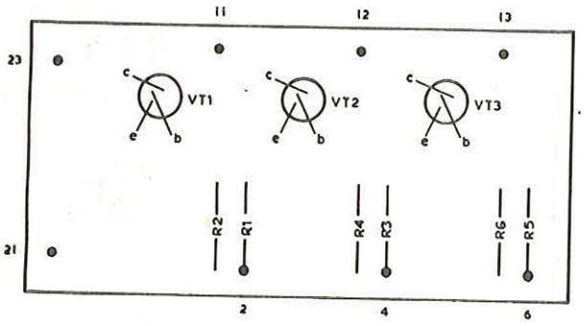


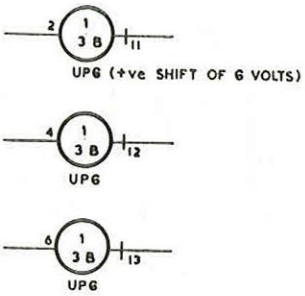


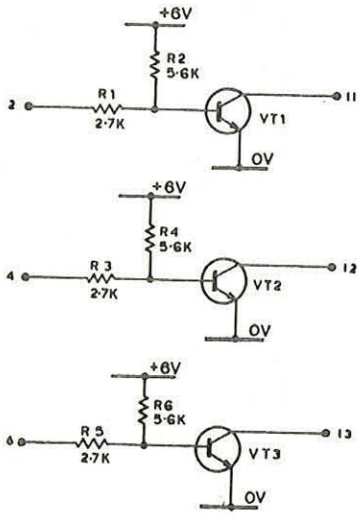


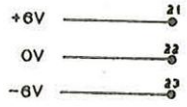
THRESHOLD VOLTAGE AT PIN 2	OUTPUT WAVEFORM PIN 13
RISING VOLTAGE +3·1V	
FALLING VOLTAGE +2·4V	

TRANSISTOR	PURCH. SPEC.	CAT. No.
VT1—VT3	PS 218	11008



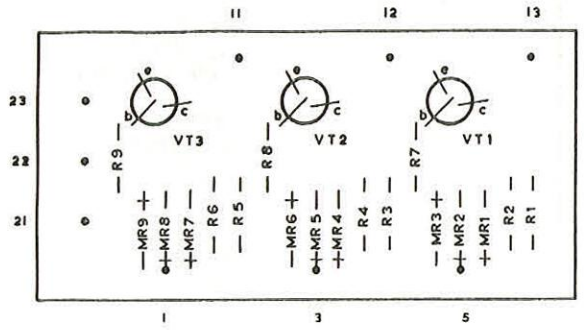


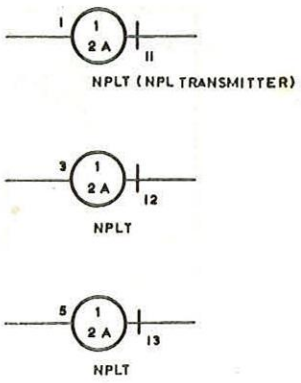


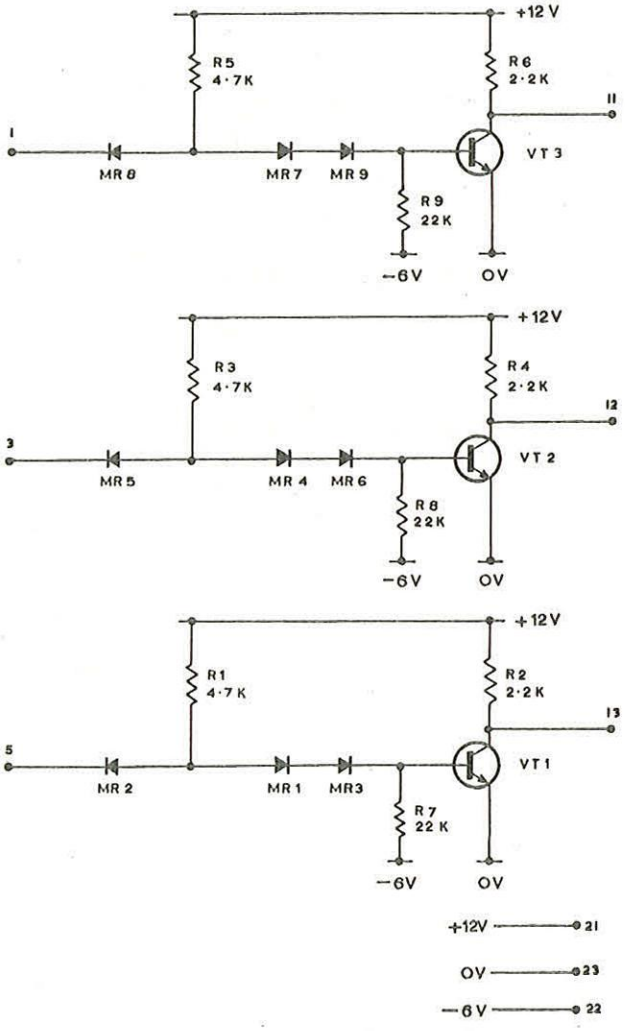


INPUT LOGIC LEVELS
'1' = > -1·2V
'0' = < -3V

TRANSISTOR	PURCH SPEC	CAT NO.
VT1 – VT3	PS 218	11008

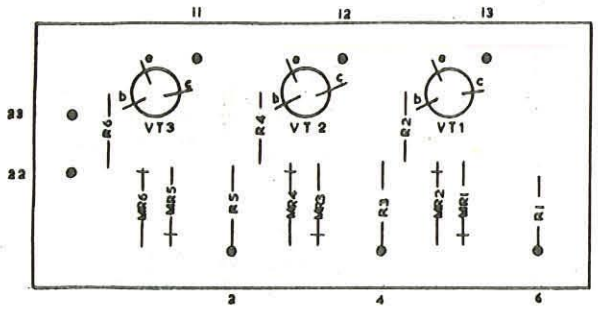


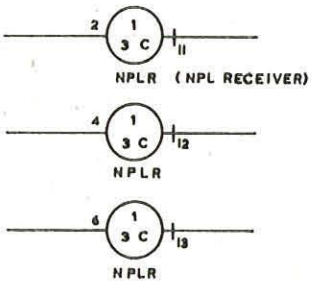


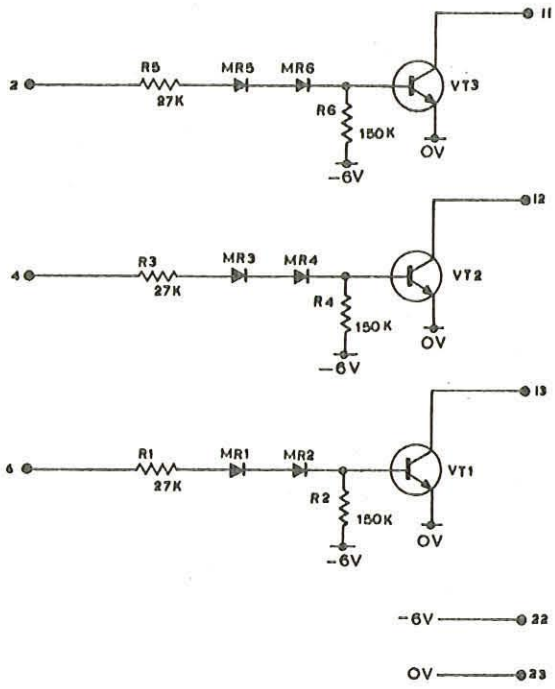


INPUT LOGIC LEVELS	
'1'	= > 2
'0'	= < 1

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1 - VT3	PS 218	11008



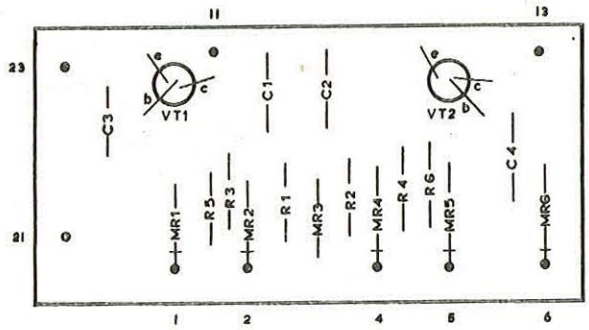


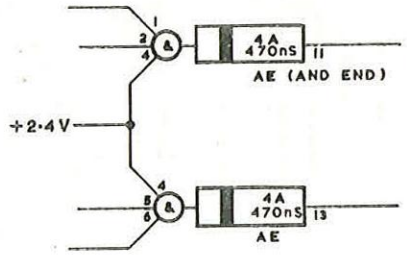


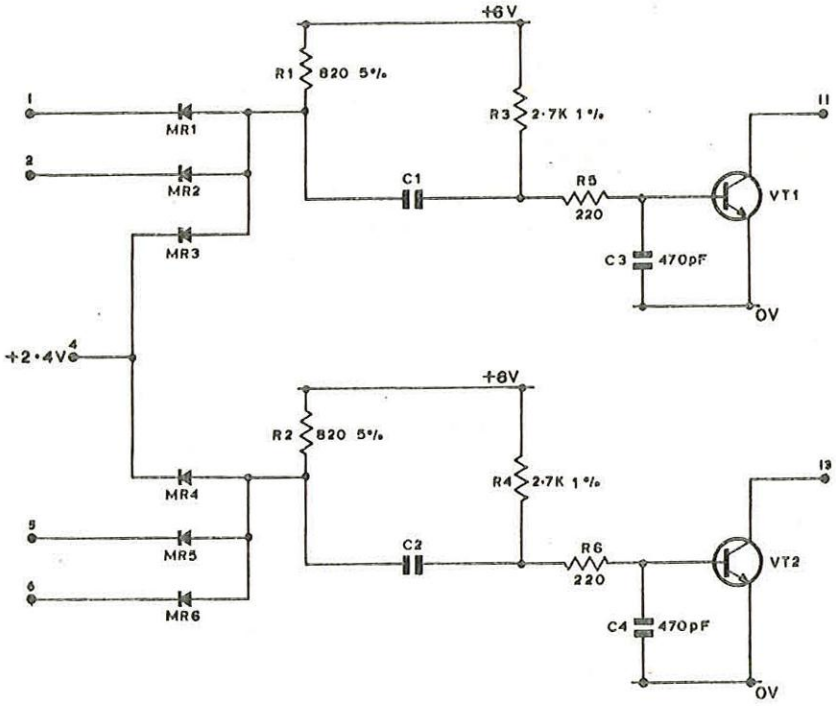
INPUT LOGIC LEVELS
"1" = > 2
'0' = < 1

Figure 35 (ISSUE 3)

TRANSISTOR	PURCH. SPEC.	CAT. No.
VT1, VT2	PS 218	11008







PULSE WIDTH = CnS (WHERE C = CAPACITANCE IN pF.)		
	UPPER ELEMENT	LOWER ELEMENT
L.S.A.	C1	C2
37	680pF	680pF
39	100pF	100pF
40	330pF	330pF
41	220pF	220pF
42	470pF	470pF

NOTES:
(1) OUTPUT PULSE POSITIVE.
(2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDED ALL I/P'S HAVE BEEN '1' FOR GREATER THAN C/2 ns. (WHERE C = CAPACITANCE IN pF.)

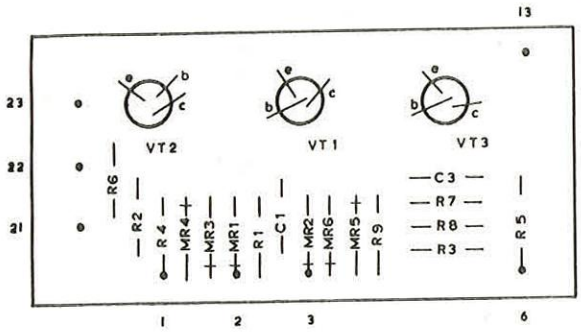
+6V ——● 21
0V ——● 23

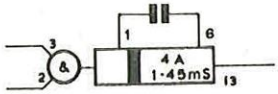
INPUT LOGIC LEVELS
'1' = > 2·4V
'0' = < 1V

Figure 36 (ISSUE 2)

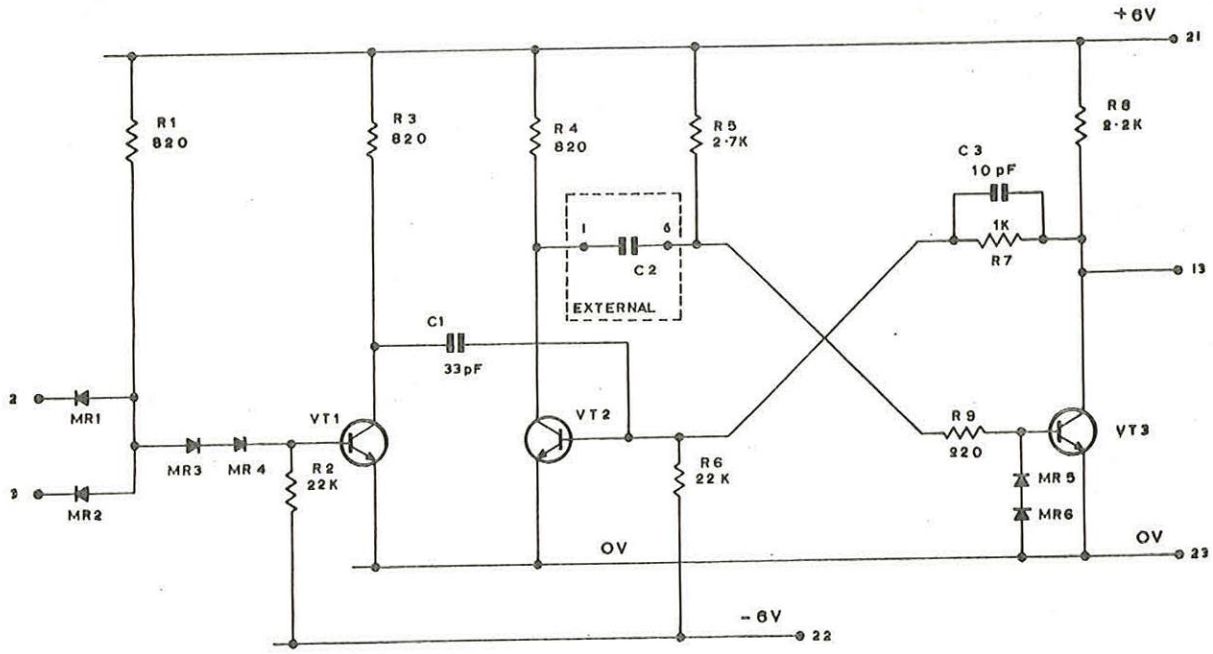
L.S.A. 37, 39, 40, 41, 42.

TRANSISTOR	PURCH. SPEC	CAT NO.
VT1-VT3	PS218	11008





AE (AND END)



NOTES:

(1) C 2 IS EXTERNAL AND SETS PULSE WIDTH

(2) OUTPUT PULSE POSITIVE

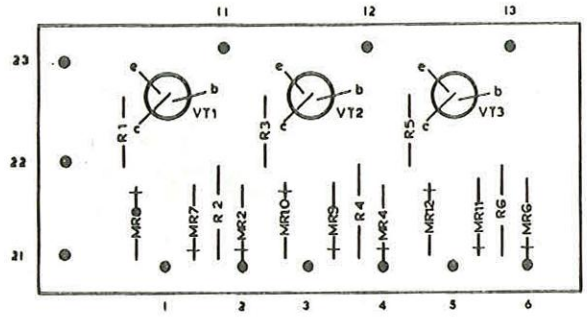
(3) PULSE TRIGGERED BY ANY INPUT REVERTING TO A '0' PROVIDED OTHER INPUT IS A '1'

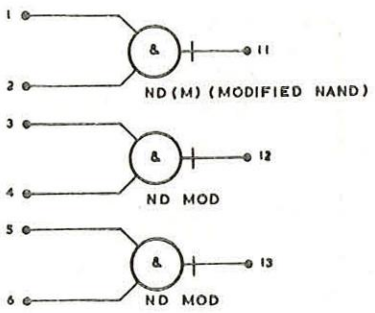
(4) PULSE WIDTH T = 1·36 × C2nS ±36 %
(WHERE C2 IS IN pF)

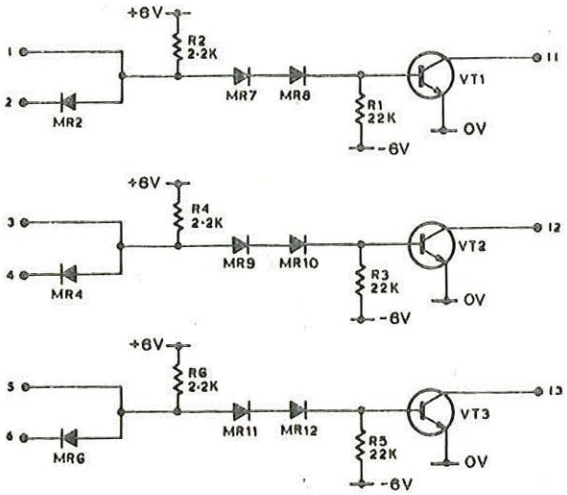
INPUT LOGIC LEVELS
'1' = >2
'0' = <1

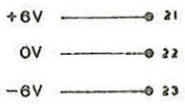
Figure 37 (ISSUE 2)

TRANSISTOR	PURCH. SPEC.	CAT. No.
VT1–VT3	PS 218	11008





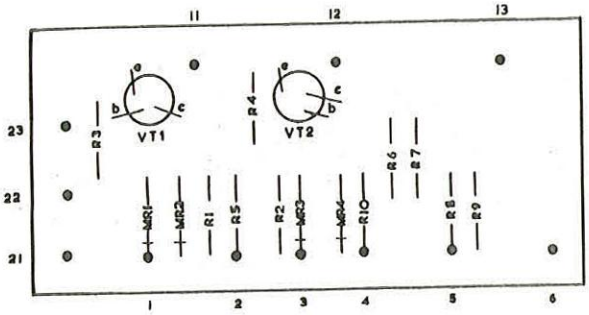


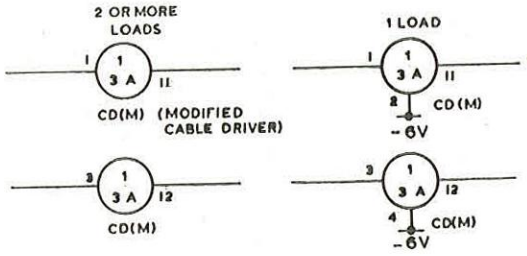


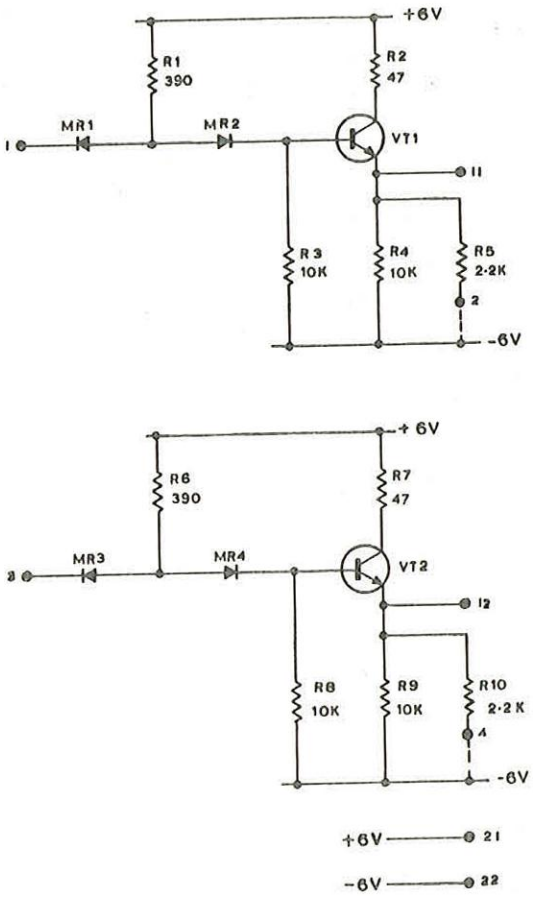
INPUT LOGIC LEVEL
'1' = > 2V
'0' = < 1V

Figure 38 (ISSUE 2)

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1 VT2	PS 218	11008



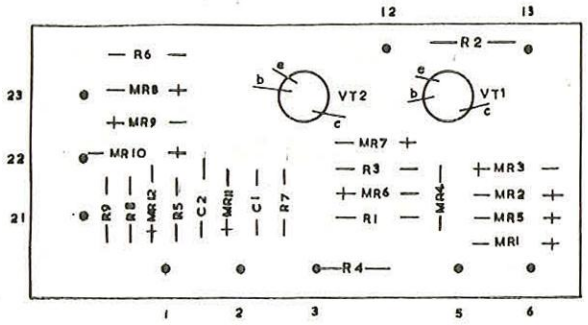


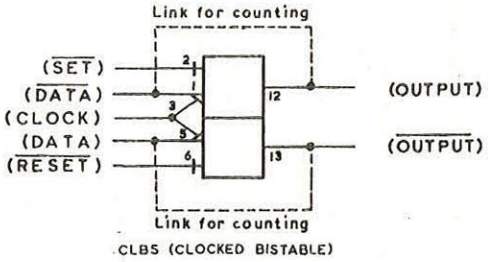


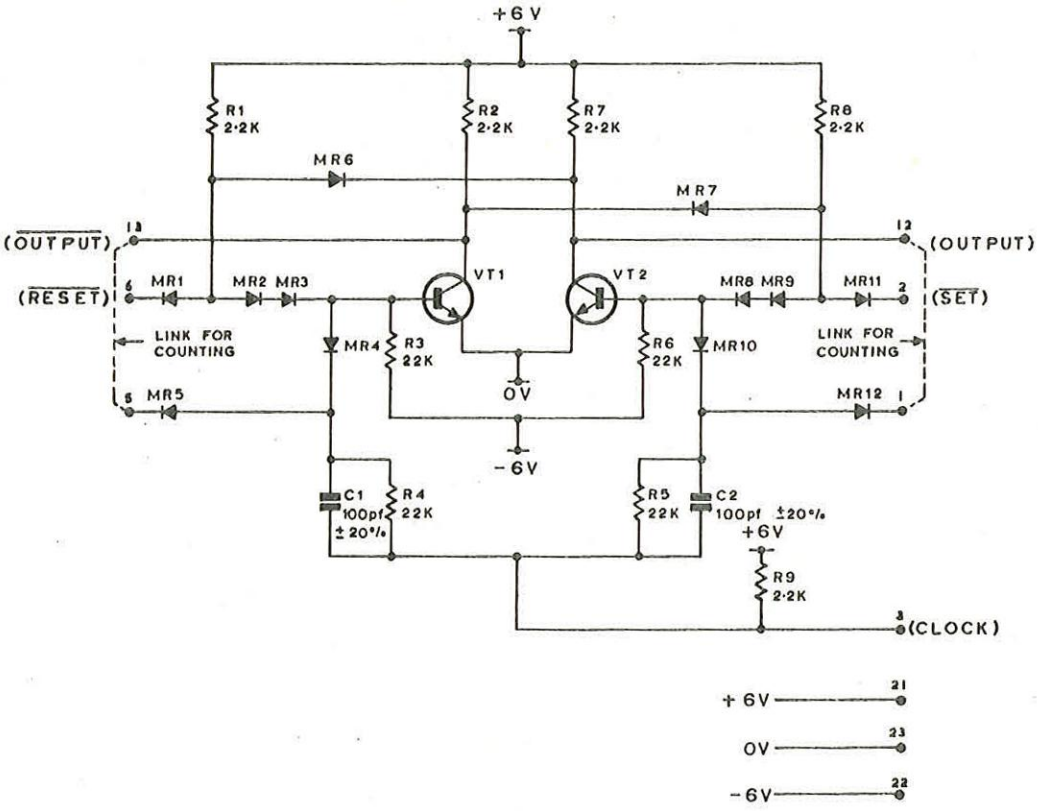
INPUT LOGIC LEVELS
'1' = > 2V
'0' = < 1V

Figure 39 (ISSUE 2)

TRANSISTOR	PURCH. SPEC.	CAT.NO.
VT1, VT2	PS218	11008



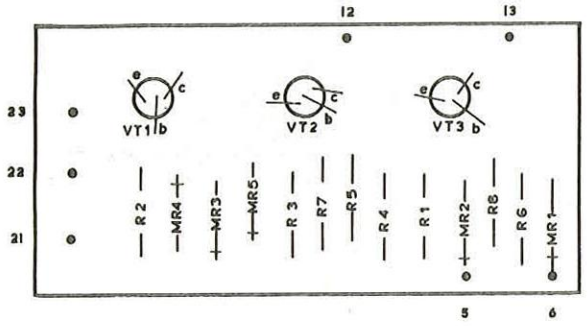


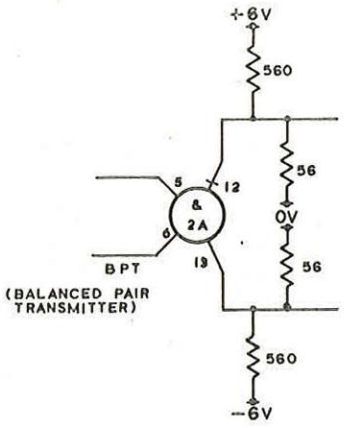


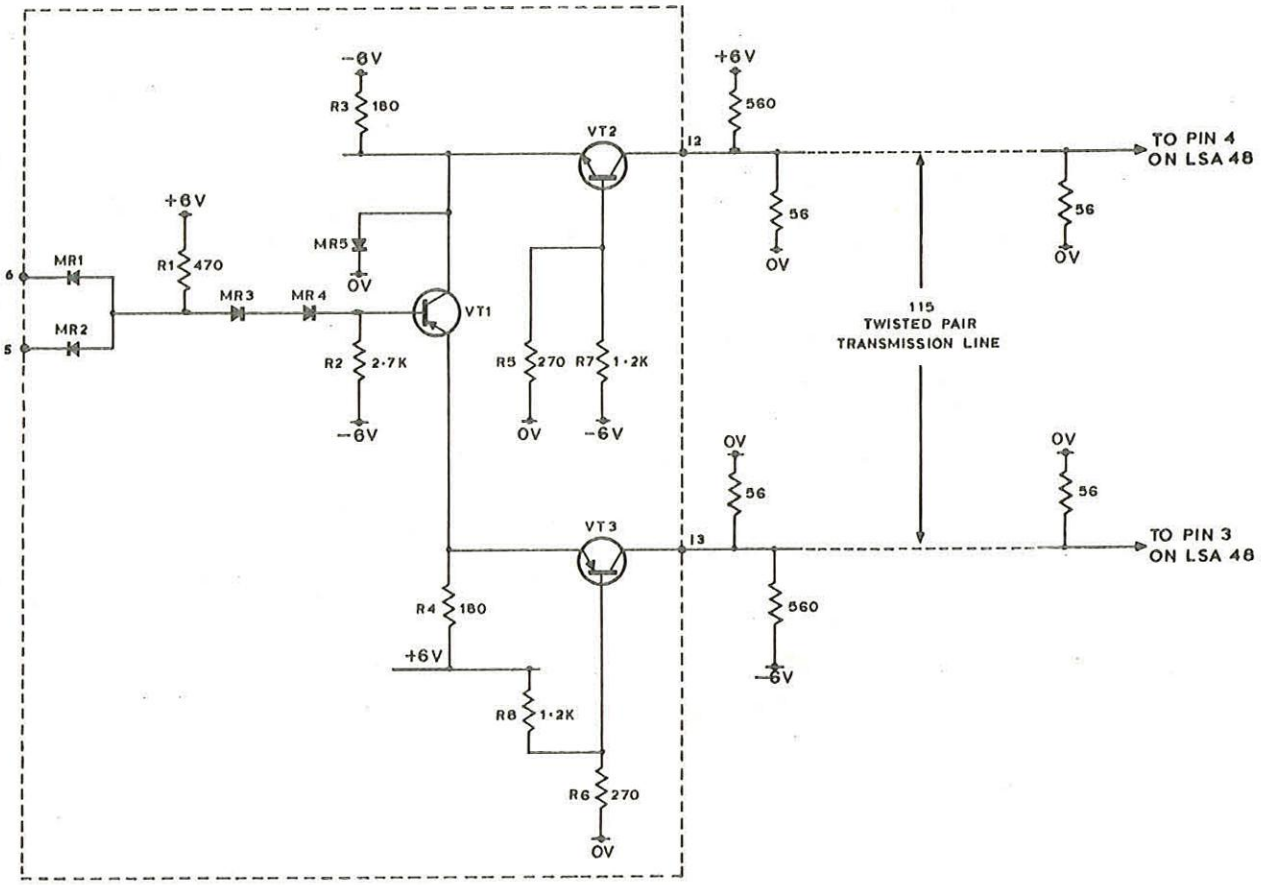
INPUT LOGIC LEVELS
'1' = > 2 V
'0' = < 1 V

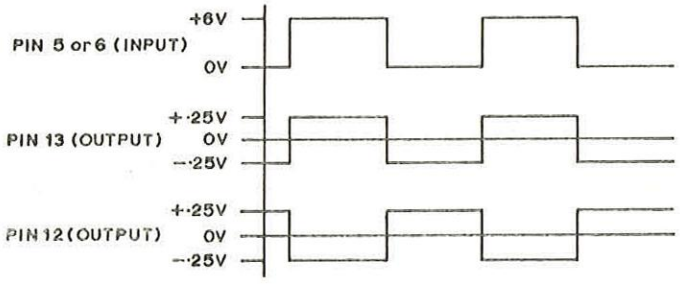
Figure 40 *(ISSUE 2)*

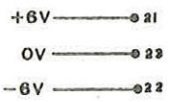
TRANSISTOR	PURCH SPEC.	CAT. No.
VT1, VT3.	PS 216.	9725.
VT2.	PS 212.	8843.







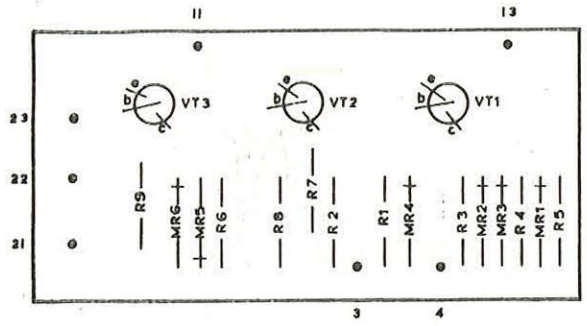


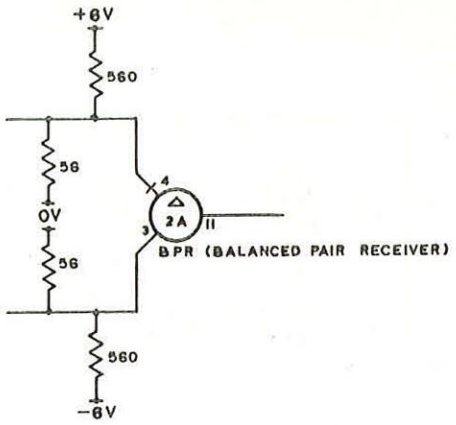


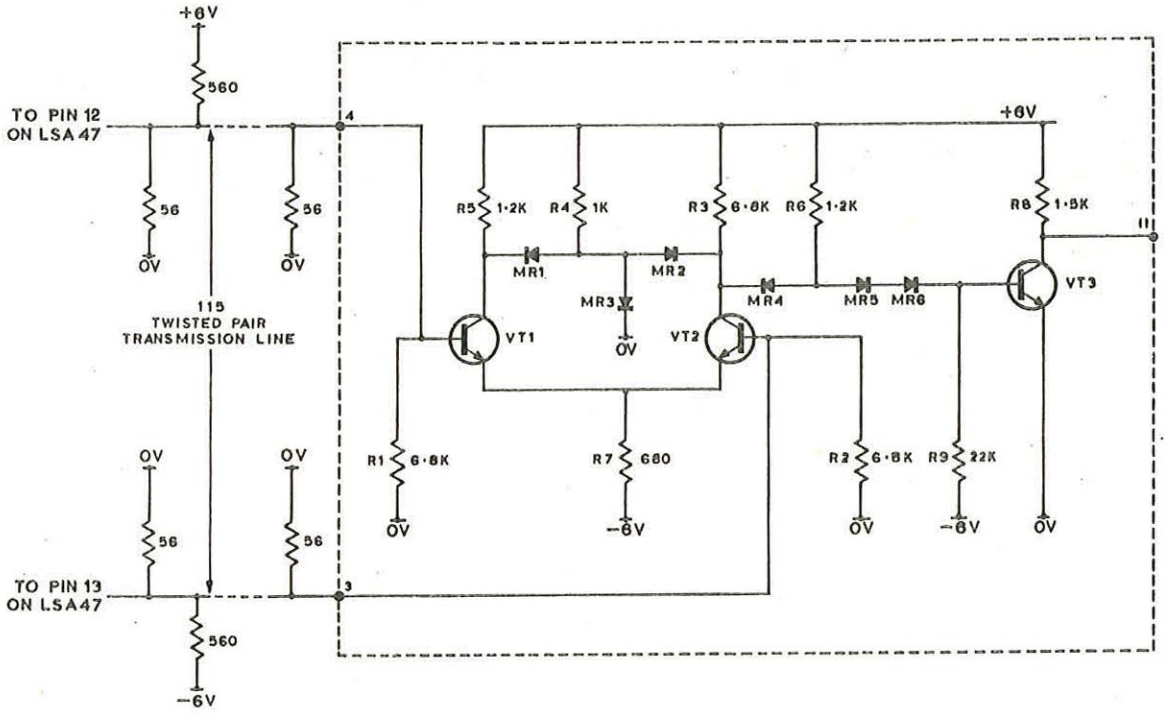
NOTE:
THE OUTPUT WAVEFORMS ABOVE ARE THOSE OBTAINED WITH TERMINATION AND BIASING AS USED ON THE CDC INTERFACE.
THE 56Ω TERMINATING RESISTORS MUST BE ON EACH END OF THE TRANSMISSION LINE.
THE 560Ω BIASING RESISTORS MAY BE AT EITHER END OF THE LINE, BUT NOT AT BOTH.

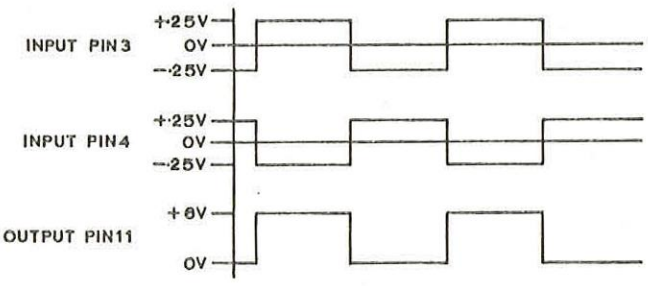
INPUT LOGIC LEVELS
'1' = > 2V
'0' = < 1V

TRANSISTOR	PURCH. SPEC.	CAT No.
VT1, VT2	PS 212	8843
VT3	PS 218	11008







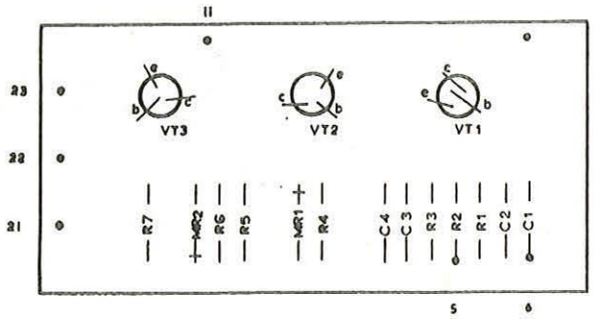


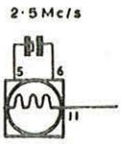
NOTE:
THE INPUT WAVEFORMS ABOVE ARE THOSE OBTAINED WITH TERMINATION AND BIASING AS USED ON THE CDC INTERFACE.
THE 56Ω TERMINATING RESISTORS MUST BE ON EACH END OF THE THE TRANSMISSION LINE.
THE 560Ω BIASING RESISTORS MAY BE AT EITHER END OF THE LINE, BUT NOT AT BOTH.

INPUT LOGIC LEVELS
'1' = PIN 4 > PIN 3 BY 0·4V MIN. 0·6V MAX.
'0' = PIN 3 > PIN 4 BY 0·4V MIN. 0·6 V MAX.

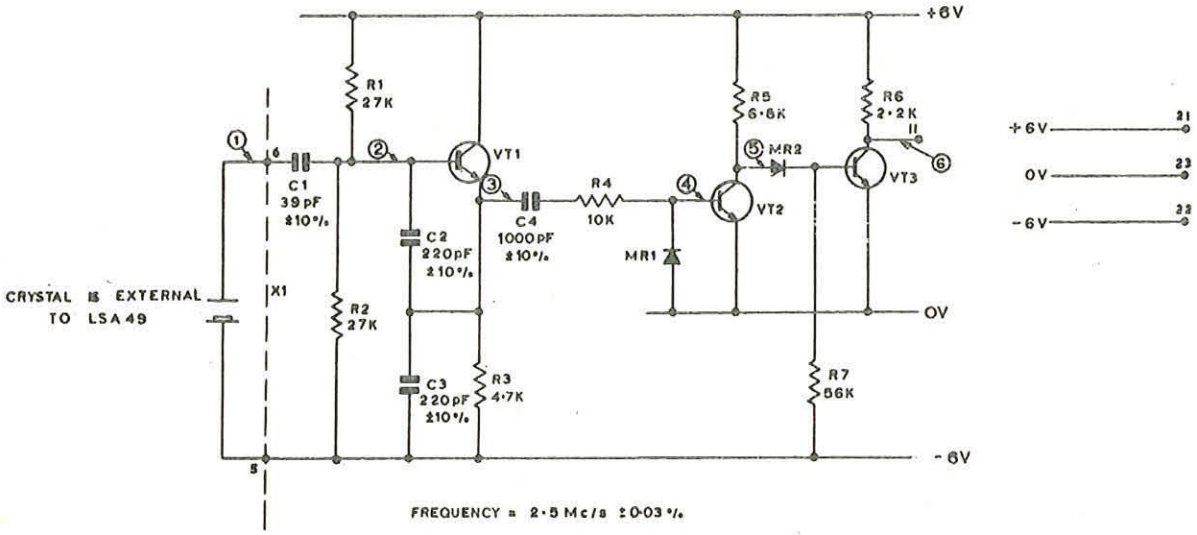
Figure 42. (ISSUE 2)

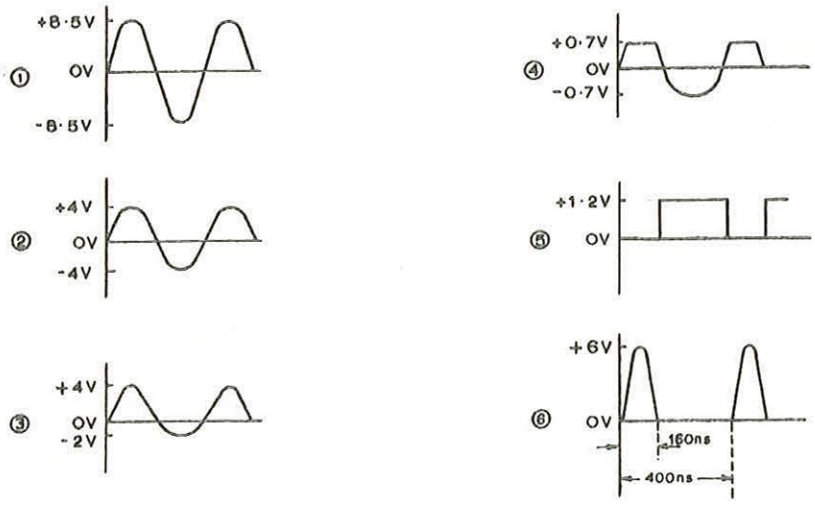
TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1	—	13053
VT2 VT3	PS218	11008



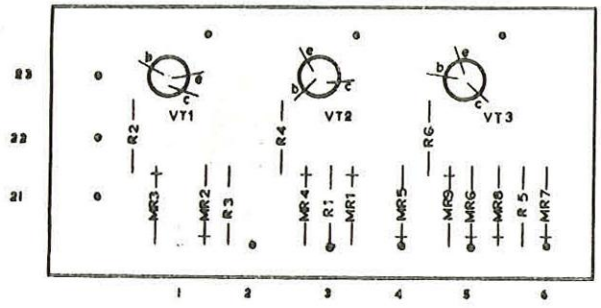


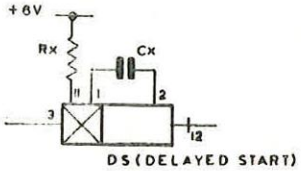
CO (CRYSTAL OSCILLATOR)

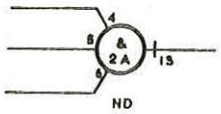


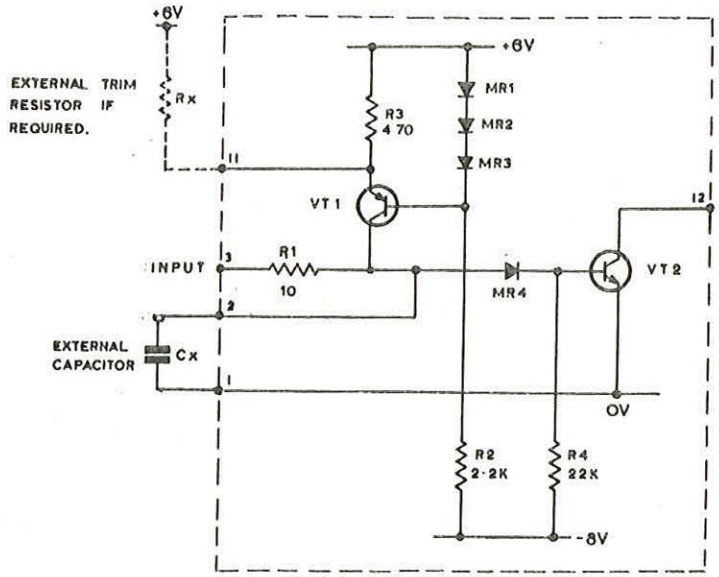


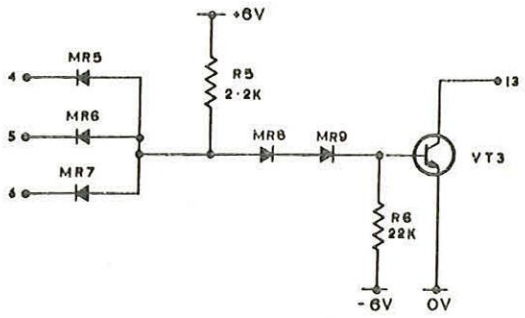
TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1	PS219	11009
VT2,VT3	PS218	11008



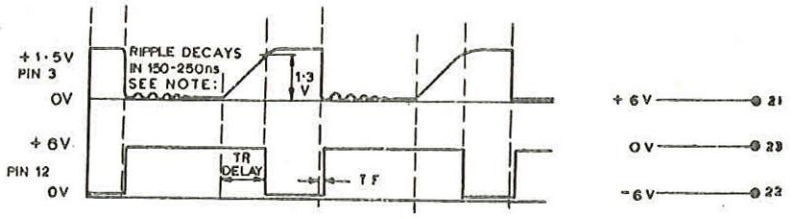








ADD:
TR = 35 + 0·44 Cx nS
(where Cx is in pF)
TF = 30 + 0·05 TR nS
(where TR is in nS)



NOTE:
1. Assuming connection to driving source is not more than 6ins long.

INPUT LOGIC LEVELS	
DELAY ELEMENT	'1' = >0·25V AT 3mA '0' = OPEN CIRCUIT
NAND GATE	'1' = >2V '0' = <1V

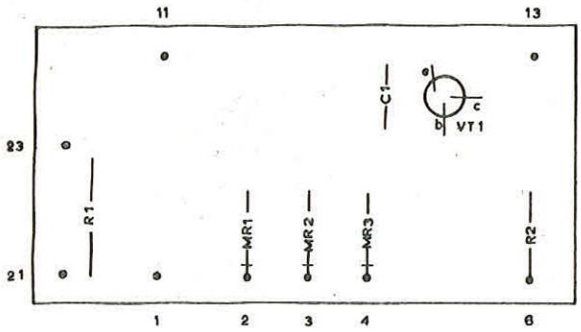
Value	Tol.	Voltage	Cat. No.	Nominal Delay
220 pf	± 5%	400V	9313	132 ± 32.9 ns.
330 pf	± 5%	400V	8479	180 ± 45.1 ns.
470 pf	± 5%	400V	7916	242 ± 60.4 ns.
680 pf	± 5%	400V	8480	334 ± 83.6 ns.
1000 pf	± 5%	400V	7917	475 ± 119 ns.
1500 pf	± 5%	400V	7924	695 ± 174 ns.
2200 pf	± 5%	400V	7918	1.00 ± 0.251 µs.
3300 pf	± 5%	400V	7919	1.49 ± 0.372 µs.
4700 pf	± 5%	125V	7920	2.10 ± 0.526 µs.
6800 pf	± 5%	125V	7921	3.03 ± 0.757 µs.
0.01 µF	± 5%	400V	7922	4.44 ± 1.11 µs.
0.015 µF	± 5%	125V	7504	6.63 ± 1.66 µs.
0.022 µF	± 5%	125V	7475	9.72 ± 2.43 µs.
0.033 µF	± 5%	125V	7720	14.6 ± 3.64 µs.
0.047 µF	± 5%	125V	7044	20.7 ± 5.18 µs.
0.068 µF	± 5%	125V	8481	30.0 ± 7.49 µs.
0.1 µF	± 5%	20V	9136	44.0 ± 11.0 µs.
0.15 µF	± 5%	20V	9915	66.0 ± 16.5 µs.
0.22 µF	± 5%	20V	11043	96.8 ± 24.2 µs.
0.33 µF	± 5%	15V	9369	145 ± 36.3 µs.
0.47 µF	± 5%	15V	NR	207 ± 51.7 µs.
0.68 µF	± 5%	15V	9430	299 ± 74.8 µs.
1.0 µF	± 5%	15V	9386	440 ± 110 µs.
1.5 µF	NR	15V	----	660 ± 165 µs.
2.2 µF	NR	15V	----	968 ± 242 µs.
3.3 µF	± 5%	15V	9431	1.45 ± 0.363 ms.
4.7 µF	± 5%	15V	9398	2.07 ± 0.517 ms.
6.8 µF	± 5%	15V	9387	2.99 ± 0.748 ms.
10.0 µF	± 5%	15V	9309	4.40 ± 1.10 ms.
15.0 µF	± 5%	15V	NR	6.60 ± 1.65 ms.
22.0 µF	± 5%	15V	9385	9.68 ± 2.42 ms.
33.0 µF	± 5%	15V	11044	14.5 ± 3.63 ms.
47.0 µF	± 5%	15V	11042	20.7 ± 5.17 ms.
68.0 µF	± 5%	15V	9308	29.9 ± 7.48 ms.
100.0 µF	± 5%	10V	9151	44.0 ± 11.0 ms.

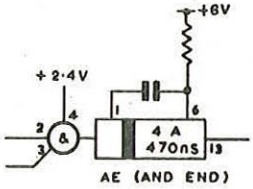
% Reduction of delay	0.99	1.4	2.1	3.0	4.5	5.4	6.5	7.7	9.1	12	18
Resistor	47K	33K	22K	15K	10K	8.2K	6.8K	5.6K	4.7K	3.3K	2.2K
% Reduction of delay	24	32	36	41	46	50	59	68	76	82	
Resistor	1.5K	1	820Ω	680Ω	560Ω	470Ω	330Ω	220Ω	150Ω	100Ω	

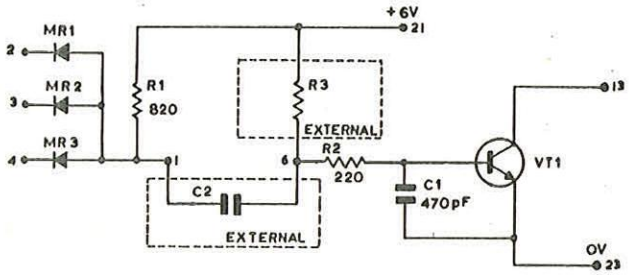
CAPACITOR SELECTION

Figure 44a (Issue 2)

TRANSISTOR	PURCH. SPEC.	CAT NO.
VT1	PS 218	11008





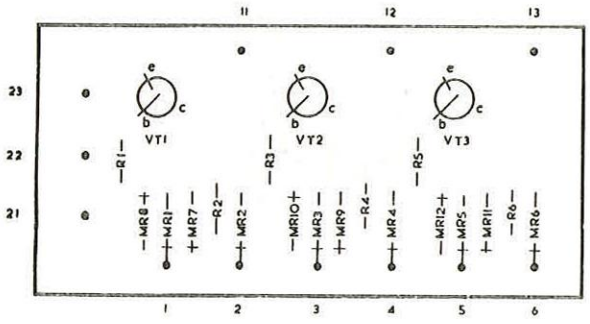


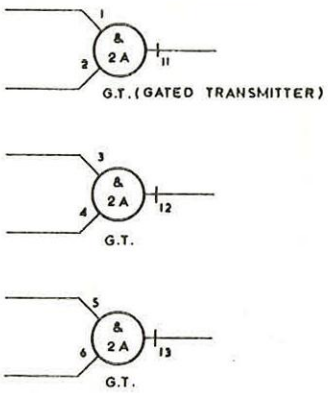
NOTES

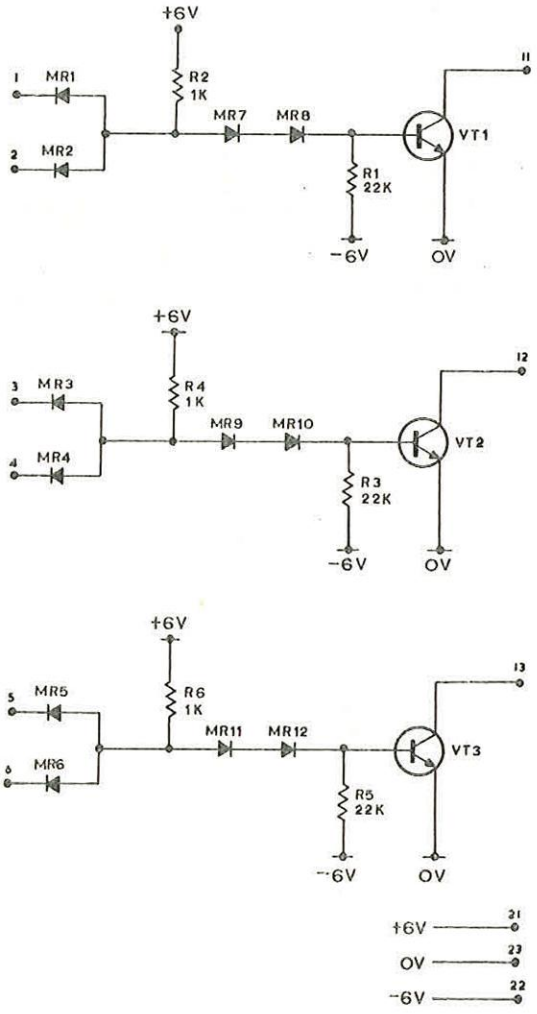
1. OUTPUT PULSE POSITIVE.
2. PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDED ALL I/P'S HAVE BEEN '1' FOR > $\frac{C}{2}$ nS.
   (WHERE C = CAPACITANCE IN pF)
3. R3 AND C2 ARE EXTERNAL.
4. IF R3 = 2·7K THEN THE PULSE WIDTH = C nS (WHERE C IS CAPACITANCE OF C2 IN pF) INCREASING VALUE OF R3 INCREASE PULSE WIDTH IN PROPORTION.

INPUT LOGIC LEVELS
'1' = > 2V
'0' = < 1V

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1-VT3	—	7573

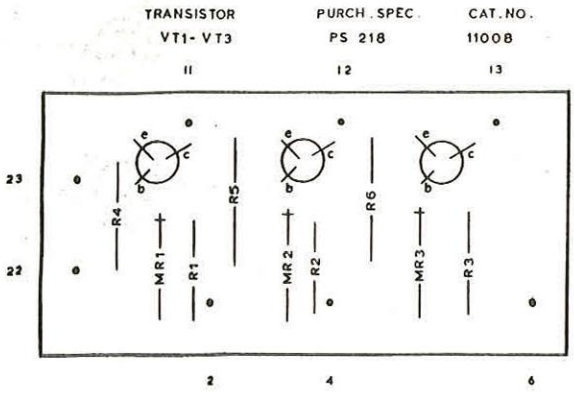


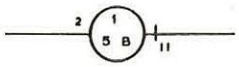




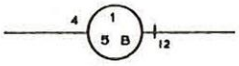
INPUT LOGIC LEVELS
'1' = > 2V
'0' = < 1V

Figure 46 (ISSUE 2)

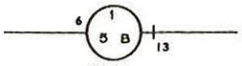




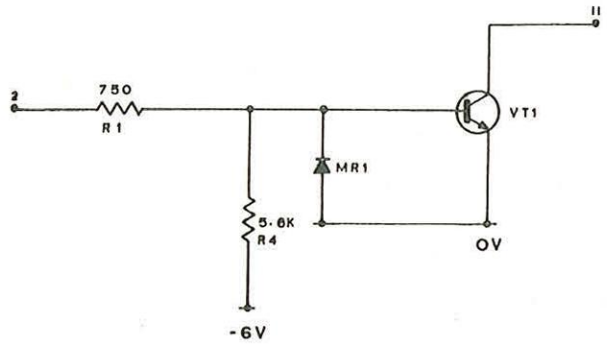
41PR (4100 PERIPHERAL RECEIVER)

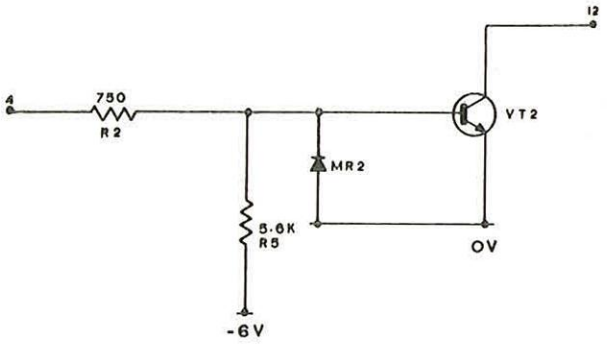


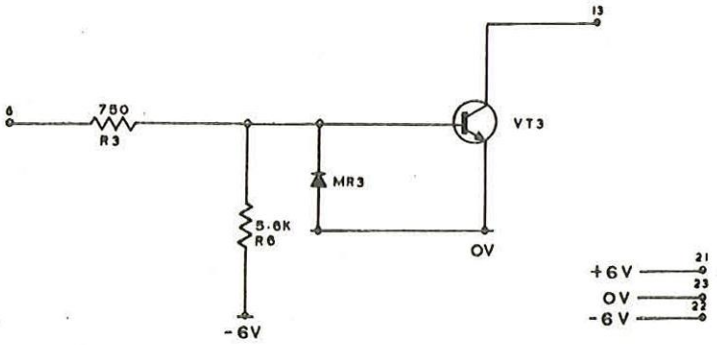
41PR



41PR



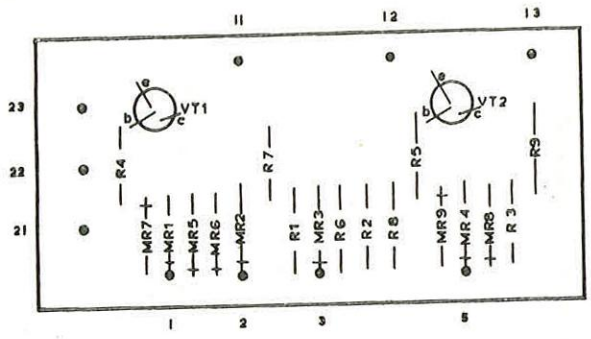


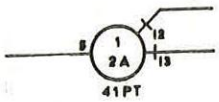


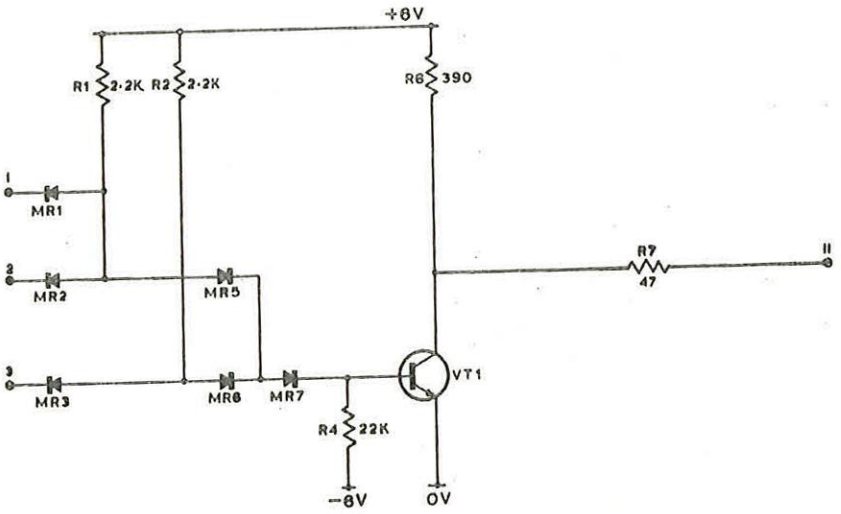
INPUT LOGIC LEVELS
'1' = > 3 V
'0' = < 1 V

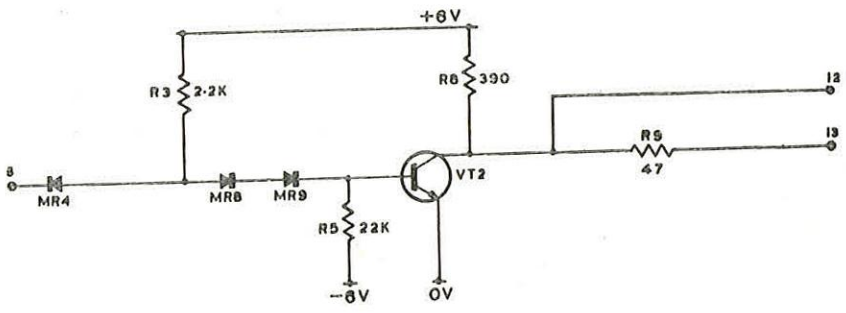
Figure 47 (ISSUE 2)

TRANSISTOR.	PURCH. SPEC.	CAT. No.
VT1, VT2.	PS 218	11008





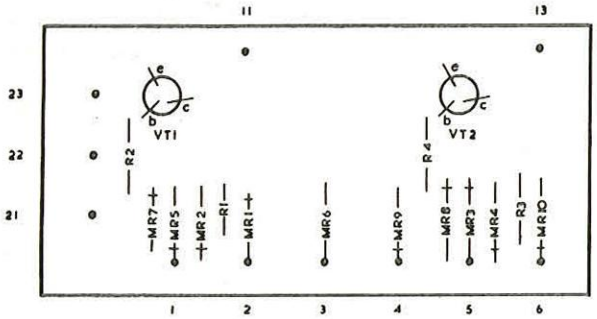


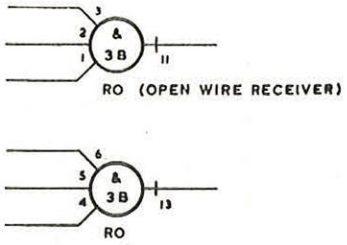


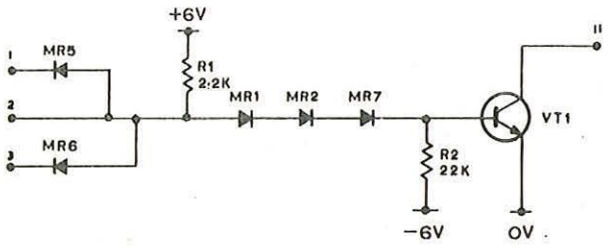
INPUT LOGIC LEVELS
↑ = > 2V
↓ = < 1V

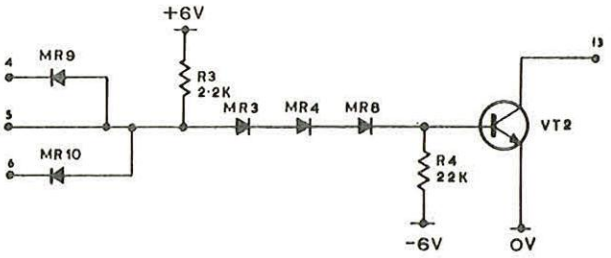
Figure 48 (ISSUE 2)

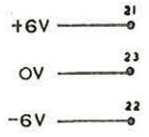
TRANSISTOR	PURCH. SPEC	CAT. NO.
VT1, VT2	PS 218	11008







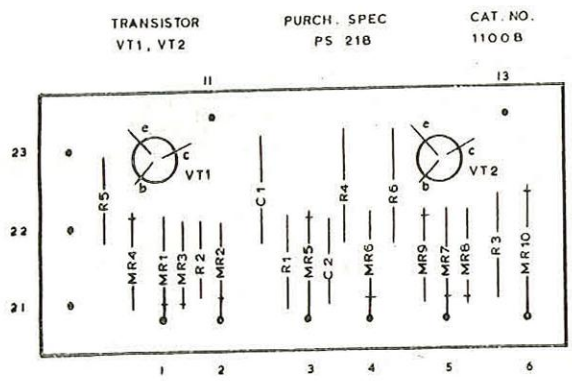


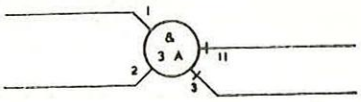


NOTE
INPUTS 1,2 AND 4,6, USED WHEN RECEIVING
FROM BUS INPUTS 2 AND 5 OTHERWISE

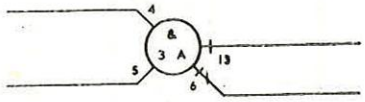
INPUT LOGIC LEVELS
'1' = > 2·8V
'0' = < 1·5V

Figure 49 (ISSUE 2)

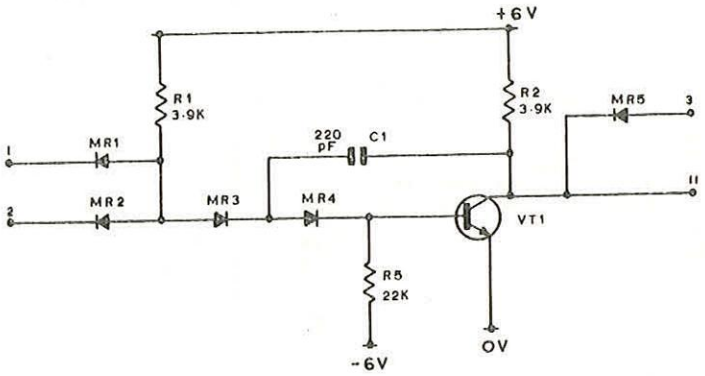


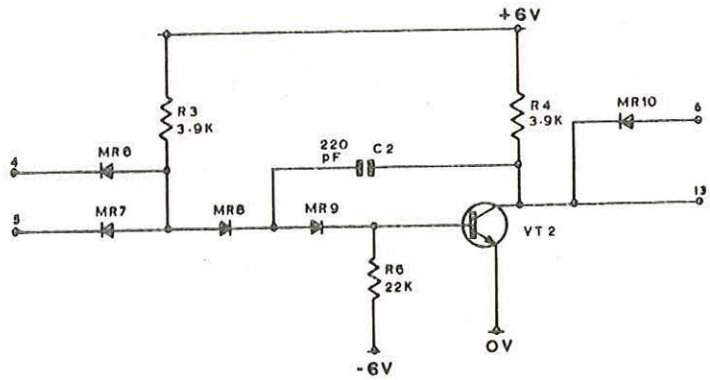


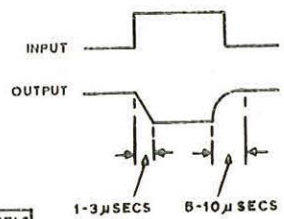
TO(OPEN WIRE TRANSMITTER)



TO





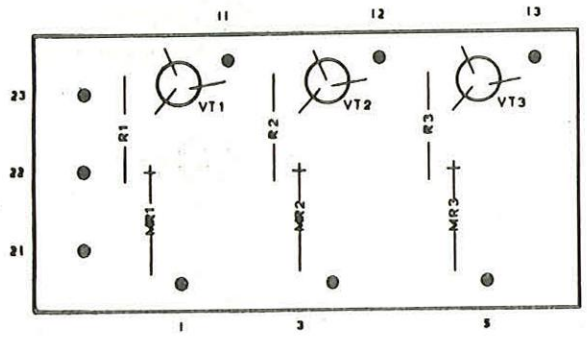


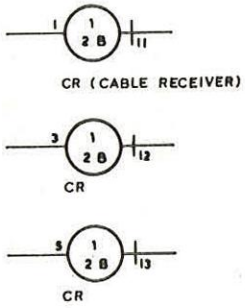
INPUT LOGIC LEVELS
'1' = > 2 V
'0' = < 1 V

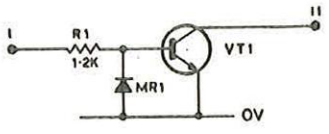
NOTE:-
OUTPUTS 3&6 USED WHEN DRIVING ON TO BUS. OUTPUTS 11&13 USED OTHERWISE.

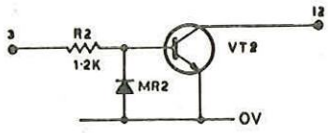
Figure 50 (ISSUE 2)

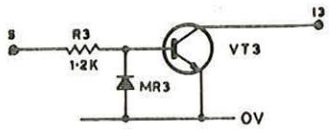
TRANSISTOR	PURCH. SPEC.	CAT. No.
VT1–VT3	PS 218	11008









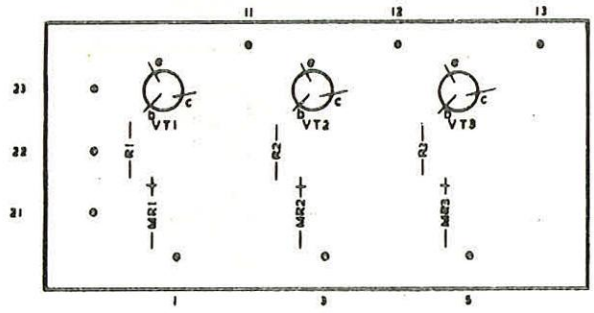


NOTE:–

USED IN CONJUNCTION WITH A SINGLE FAST CABLE DRIVER LSA12G FEEDING BUS OF RECEIVERS.

INPUT LOGIC LEVELS
'1' ≡ > 2V
'0' ≡ < 1·5V

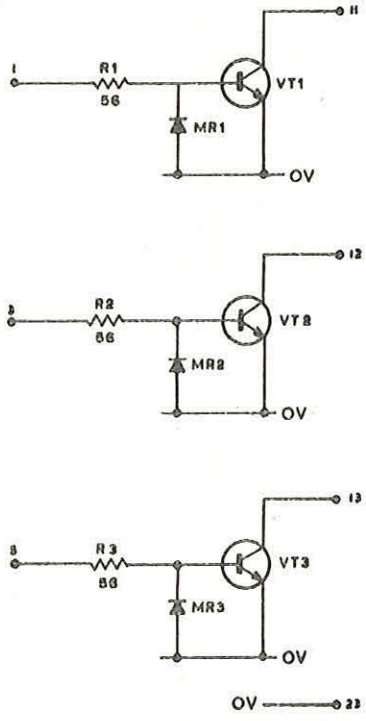
TRANSISTOR	PURCH. SPEC.	CAT NO.
VT1–VT3	PS 218	11008



CR (CABLE RECEIVER)

CR

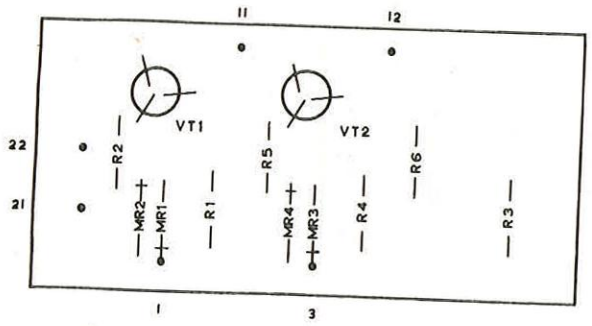
CR

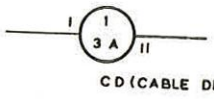


NOTE:
USED IN CONJUNCTION WITH A BUS OF FAST CABLE DRIVERS L.S.A. 126 FEEDING A SINGLE RECEIVER.

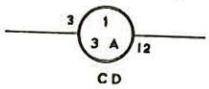
INPUT LOGIC LEVELS
'1' = > 2V
'0' = < 1·5V

TRANSISTOR	PURCH. SPEC	CAT NO.
VT1, VT2	PS 218	11008

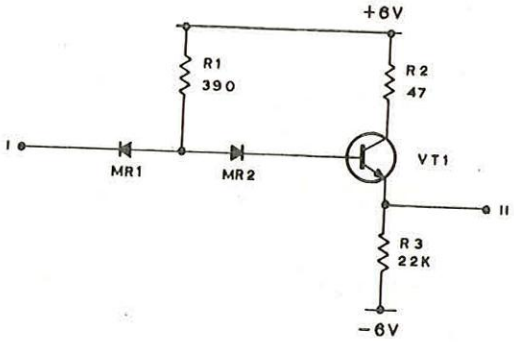


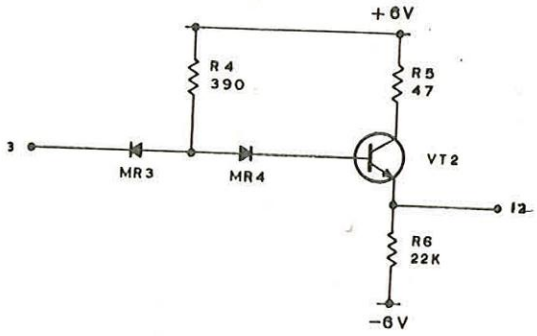


CD (CABLE DRIVER)



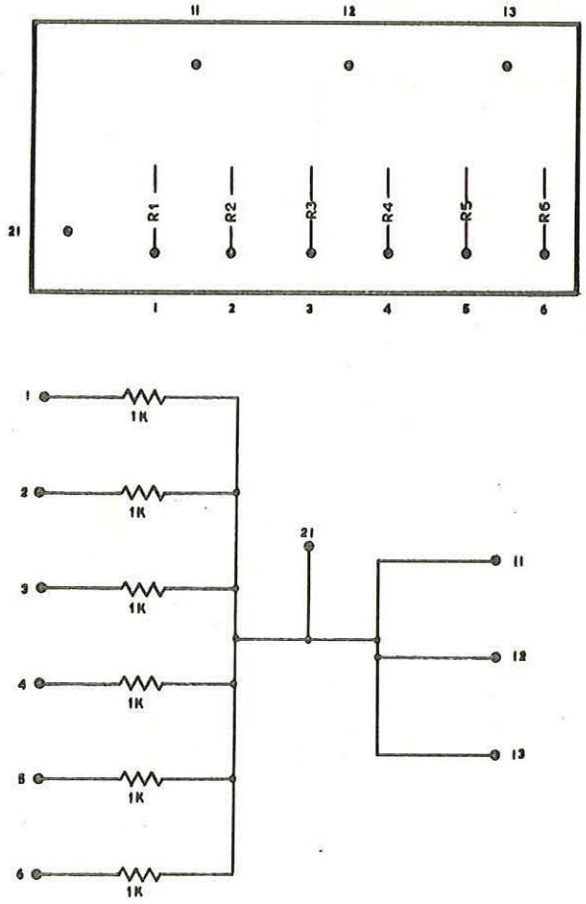
CD



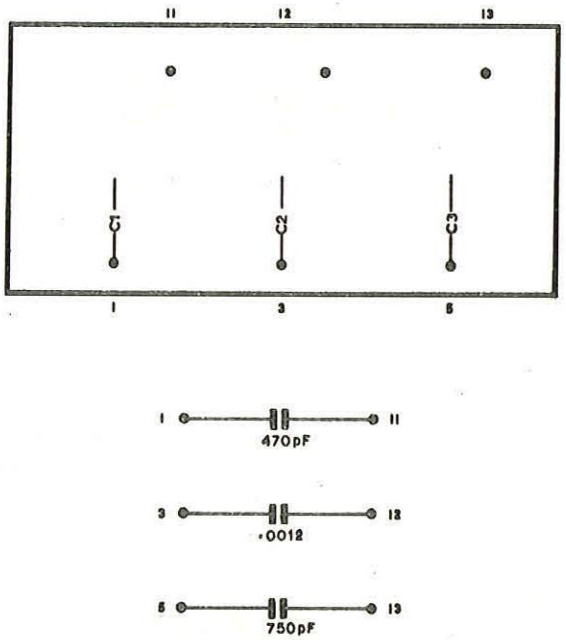


INPUT LOGIC LEVELS
'1' = >3·5V
'0' = < 1V

Figure 53 (ISSUE 2)



L.S.A. 132

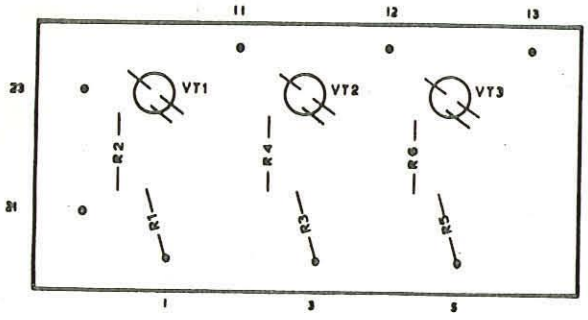


L.S.A.133

Figure 54 (ISSUE 2)

L.S.A.132 & L.S.A.133

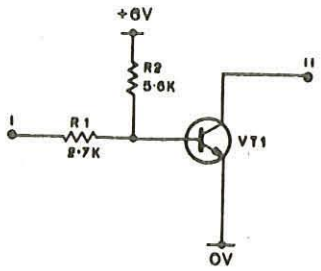
TRANSISTOR	CAT. No.
VT1 – VT3	11740

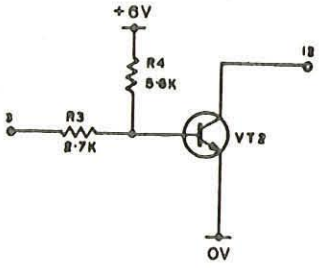


LSH/136 (LEVEL SHIFTER LSA136)

LSH/136

LSH/136





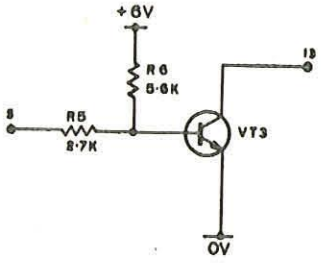


Figure 55 (ISSUE 2)